ACADEMIC REGULATIONS (R20)

COURSE STRUCTURE AND DETAILED SYLLABUS

(CHOICE BASED CREDIT SYSTEM (CBCS))

MASTER OF TECHNOLOGY
IN
VLSI

For

M. Tech. - Regular Two Year Post Graduate Degree Programme

(Applicable for the batches admitted from 2020 - 2021)

CMR INSTITUTE OF TECHNOLOGY

(UGC - Autonomous)

Approved by AICTE, Permanently Affiliated to JNTUH, Accredited by NAAC with A Grade and NBA

Kandlakoya(V), Medchal District, Hyderabad-501 401, Telangana State

Landline: 08418-200720; Fax: 08418-200240

E-mail: principal@cmritonline.ac.in Web: www.cmritonline.ac.in

FOREWORD

CMR Institute of Technology, established in the year 2005, Approved by AICTE, New Delhi, Permanently Affiliated to JNTUH, twice Accredited by NBA, Achieved UGC Autonomous Status and has been bestowed with NAAC 'A' Grade in July 2018 for its remarkable academic accomplishments accompanied by its unflinching spirit and dedication to impart quality technical education to the deserving aspirants. The institution has commenced functioning independently within the set norms prescribed by UGC and AICTE. The performance of the institution manifests the confidence that the prestigious monitoring body, the UGC has on it, in terms of upholding its spirit and sustenance of the expected standards of functioning on its own consequently facilitating the award of degrees for its students. Thus, an autonomous institution is provided with the necessary freedom to have its own **curriculum, examination system and monitoring mechanism**, independent of the affiliating University but under its observance.

CMR Institute of Technology takes pride for having won the confidence of such distinguished academic bodies meant for monitoring the quality in technology education. Besides, the institution is delighted to sustain the same spirit of discharging the responsibilities that it has been conveying since a decade to attain the current academic excellence, if not improving upon the standards and ethics. Consequently, statutory bodies such as the Academic Council and the Boards of Studies have been constituted under the supervision of the Governing Body of the College and with the recommendations of the JNTU Hyderabad, to frame the regulations, course structure and syllabi for autonomous status.

The autonomous regulations, course structure and syllabi have been framed in accordance with the vision and mission of the institution along with certain valuable suggestions from professionals of various ancillary fields such as the academics, the industry and the research, all with a noble vision to impart quality technical education and contribute in catering full-fledged engineering and management graduates to the society.

All the faculty members, the parents and the students are requested to study all the rules and regulations carefully and approach the Principal to seek any clarifications, if needed, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the institution and for brightening the career prospects of engineering and management graduates.

CMR INSTITUTE OF TECHNOLOGY

Vision: To create world class technocrats for societal needs.

Mission: Impart global quality technical education for a better future by providing appropriate learning environment through continuous improvement and customization.

Quality Policy: Strive for global excellence in academics & research to the satisfaction of students and stakeholders.

Department of Electronics & Communication Engineering (ECE)

Vision: To be a centre of excellence in the field of electronics and communication engineering where learners are nurtured in a scholarly environment to meet global challenges.

Mission: Provide conducive environment to hone up the learners' technical skills by imparting quality education in the field of electronics and communication engineering to fulfill societal needs.

M.Tech. - Regular Two Year Post Graduate Degree Programme

(For batches admitted from the academic year 2020 - 21)

PREAMBLE

For pursuing M.Tech. - Regular Two Year Post Graduate Degree Programme offered by **CMR Institute of Technology (CMRIT)** under Autonomous status will herein be referred to as CMRIT (Autonomous).

All the specified rules are herein approved by the Academic Council. These rules will be in force and are applicable to students admitted from the academic year 2020-21 onwards. Any reference to "**Institute**" or "**College**" in these rules and regulations stand for CMRIT (Autonomous).

All the rules and regulations specified shall hereafter be read as a whole for the purpose of interpretation, as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, CMRIT (Autonomous) shall be The Chairman, Academic Council.

1. POST GRADUATE PROGRAMS OFFERED

CMR Institute of Technology, an autonomous college affiliated to JNTUH, offers M.Tech. - Regular 2 years (4 semesters) Post Graduate Degree Programme, under Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) are taken as 'references' for the present set of Regulations with effect from the academic year 2020 - 21 onwards. The following specializations are offered at present for the M. Tech. programme of study.

Sl. No.	Programme	Offering Department
1	Structural Engineering	Civil Engineering
2	CAD/CAM	Mechanical Engineering
3	VLSI System Design	Electronics & Communication Engineering
4	Computer Science and Engineering	Computer Science and Engineering

2. ADMISSION CRITERIA AND MEDIUM OF INSTRUCTION

2.1. Admission into first year of M.Tech. - Regular Two Year Post Graduate Degree Programme

2.1.1 Eligibility: A candidate seeking admission into the first year of M.Tech. shall be made subject to eligibility and qualification as prescribed by the university from time to time. Admissions shall be made on the basis of merit/rank obtained by the candidate qualified at TSPGECET/GATE or any entrance test conducted by the university or on the basis of any other order of merit as approved by the university, subject to reservations as laid down from time to time by government of Telangana.

2.1.2 Admission Procedure: Admissions are made into the first year M.Tech. as per the stipulations of the TSPGECET/GATE.

(a) Category A: 70% seats are filled through TSPGECET/GATE counseling.
(b) Category B: 30% seats are filled by the management.

2.2. College Transfers: There shall be no college transfers after the completion of admission process.

2.3. Medium of Instruction: The medium of instruction and examinations for the entire M.Tech. - Programme will be in **English** only.

3. M.Tech. PROGRAMME (PGP in E&T) STRUCTURE

3.1 Admitted under M.Tech. (PGP in E&T) - Regular Two Year Post Graduate Degree Programme:

3.1.1 A student after securing admission shall pursue the post graduate programme in M.Tech. Programme for a minimum period of two academic years (4 semesters), and a maximum period of four academic years (8 semesters) starting from the date of commencement of first year first semester, failing which he/she shall forfeit his/her seat in M.Tech. Programme.

3.1.2 I Year is structured to provide typically 18 Credits in each of the I and II Semesters, and II Year 16 credits in each of the III & IV semesters, totaling to 68 Credits for the entire M.Tech. Programme.

3.1.3 Each student shall secure 68 credits (with CGPA ≥ 5) required for the completion of the post graduate programme and award of the M.Tech. Degree.

3.2 **UGC/AICTE** specified definitions / descriptions are adopted appropriately for various terms and abbreviations used in these academic regulations/ norms, which are listed below.

3.2.1 Semester Scheme:

M.Tech. (Regular) Programme is of 2 academic years (4 semesters) with the each academic year being divided into two semesters. Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per Semester and shall have 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)', Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) as indicated by UGC and curriculum/course structure as suggested by AICTE / JNTUH. The terms 'SUBJECT' and 'COURSE' imply the same meaning here and refer to 'Theory Subject', or 'Lab Course', or 'Design / Drawing Subject', or 'Mini Project with Seminar', or 'Dissertation', as the case may be.

3.2.2 Credit Courses:

a) All subjects/courses are to be registered by a student in a semester to earn credits. Credits shall be assigned to each subject/course in a L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods: Credits) structure, based on the following general pattern.

Theory		Practical	
1 Hr. Lecture (L) per week	1 credit	1 Hr. Practical (P) per week	0.5 credit
1 Hr. Tutorial (T) per week	1 credit	2 Hrs Practical (Lab) per week	1.0 credit

All Mandatory Courses, Study Tour, Guest Lecture, etc., will not carry any Credits.

3.2.3 Subject/ Course Classification:

The College has followed the guidelines issued by AICTE/UGC. All Subjects/Courses offered for the PGP in E&T are broadly classified as Program Core, Program Elective, Open Elective, Audit Course, Minor Course and Mini Project with Seminar, Industrial Training and Dissertation.

3.2.4 Course Nomenclature:

The Curriculum Nomenclature or Course-Structure Grouping for the M.Tech. Degree Programmes is as listed below:

S. No.	*Broad Course Classification*	*Course Group/ Category*	*Courses Description*
	Core Courses (CoC)	PC- Program Core	Includes core subjects related to the Parent Discipline/ Department/ Branch of Engineering.
		Dissertation	M.Tech. Project or PG Project or PG Major Project
		Mini Project with Seminar	Seminar based on core contents related to parent discipline/department/branch of Engineering
		Minor Courses	1 or 2 Credit courses
		Audit Courses	Mandatory courses (non credit)
	Elective Courses (EℓC)	PE– Program Electives	Includes Elective subjects related to the Parent Discipline/ Department/ Branch of Engineering.
		OE-Open Electives	Elective subjects which include inter-disciplinary subjects in an area outside the parent discipline/ department/ branch of Engineering

* **Students are encouraged to go to Industrial Training/Internship for at least 4 - 6 weeks during semester break.**

4. COURSE REGISTRATION

4.1 A **'Faculty Advisor or Counselor'** shall be assigned to each student, who advises the student about the M.Tech. Programme, its course structure and curriculum, choice / option for subjects / courses, based on his/her competence, progress, pre-requisites and interest of the students.

4.2 A Student may be permitted to Register for Subjects / Courses of 'his/her CHOICE' with a typical total of 18 Credits per Semester in I Year (Minimum being 15 Credits and Maximum being 21 Credits, permitted deviation being ±15%), and 16 Credits (inclusive of Project) per III Semester in II Year (Minimum being 14 Credits and Maximum being 21 Credits), 16 credits (inclusive of Project) per IV Semester in II Year (minimum being 16 Credits and maximum 21 Credits), based on his interest, competence, progress, and 'Pre-Requisites' as indicated for various Subjects/ Courses, in the Department Course Structure (for the relevant Specialization) and Syllabus contents for various Subjects/ Courses.

4.3 Choice for 'additional Subjects / Courses' in any Semester (above the typical 18/16 Credit norm, and within the Maximum Permissible Limit of 21/21 Credits, during I/ II Years as applicable) must be clearly indicated in the Registration, which needs the specific approval and signature of the Faculty Advisor/ Counselor on hard-copy.

4.4 Dropping of Subjects/ Courses in any Semester of I Year may be permitted, ONLY AFTER obtaining prior approval and signature from the Faculty Advisor (subject to retaining a minimum of 15 Credits), 'within 15 Days of Time' from the beginning of the current Semester.

4.5 **Core Electives**: Students have to choose five core electives as per the course structure.

4.6 **Open Electives**: Students have to choose open elective other than parent department as per the course structure.

4.7 **Project work registration:** The Project shall start immediately after the completion of I year II semester. Every Student must compulsorily register for his/her M.Tech. Project Work. The student registered for the Project work shall work for two semesters.

5. ATTENDANCE REQUIREMENTS

The programmes are offered based on a unit system with each subject being considered a unit. Attendance is calculated separately for each subject.

5.1 Attendance in all classes (Lectures / Laboratories) is compulsory. The minimum required attendance in each theory subject (***also mandatory (audit) courses***) excluding the attendance of mid-term examination is 75%. A student shall not be permitted to appear for the Semester End Examinations (SEE), if his attendance is less than 75%.

5.2 A student's Seminar report and presentation on Mini Project shall be eligible for evaluation, only if he ensures a minimum of 75% of his attendance in Seminar presentation classes on Mini Project during that Semester.

5.3 **Condoning of shortage of attendance** (between 65% and 75%) up to a maximum of 10% (considering the days of attendance in sports, games, NCC, NSS activities and Medical grounds) in each subject (Theory / Lab / Mini Project with Seminar) of a semester shall be granted by the College Academic Committee on genuine reasons.

5.4 A prescribed fee per subject shall be payable for condoning shortage of attendance after getting the approval of College Academic Committee for the same. The College Academic Committee shall maintain relevant documents along with the request from the student.

5.5 Shortage of Attendance below 65% in any subject shall in **no case be condoned.**

5.6 A Student, whose shortage of attendance is not condoned in any Subject(s) (Theory / Lab / Mini Project with Seminar) in any Semester, is considered as 'Detained in that Subject(s), and is not eligible to write Semester End Examination(s) of such Subject(s), (in case of Mini Project with Seminar, his/her Mini Project with Seminar Report or Presentation are not eligible for evaluation) in that Semester; and he/she has to seek re-registration for those Subject(s) in subsequent Semesters, and attend the same as and when offered.

5.7 A student fulfills the attendance requirement in the present semester, shall not be eligible for readmission into the same class.

5.8 **a)** A student shall put in a minimum required attendance in at least **three theory subjects (excluding *mandatory (audit)* course)** in first Year I semester for promotion to first Year II Semester.

b) A student shall put in a minimum required attendance in at least **three theory subjects (excluding *mandatory (audit)* course)** in first Year II semester for promotion to second Year I Semester.

6. ACADEMIC REQUIREMENTS

The following academic requirements have to be satisfied, in addition to the attendance requirements mentioned in item no. 5.

6.1 A Student shall be deemed to have satisfied the Academic Requirements and earned the Credits allotted to each Subject/ Course, if he secures not less than 40% Marks (28 out of 70 Marks) in the End Semester Examination, and a minimum of 50% of Marks in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of Letter Grades, this implies securing B Grade or above in that Subject.

6.2 A Student shall be deemed to have satisfied the academic requirements and earned the Credits allotted to - Mini Project with Seminar, if student secures not less than 50% of the total Marks to be awarded. The Student would be treated as failed, if the student -

(i) does not present the Mini Project with Seminar as required, or
(ii) Secures less than 50% of Marks (< 50 Marks) in Mini Project with Seminar.

6.3 A Student shall - register for all Subjects covering 68 Credits as specified and listed in the Course Structure for the chosen PGP Specialization, put up all the Attendance and Academic requirements for securing 68 Credits obtaining a minimum of B Grade or above in each Subject and 'earn all 68 Credits securing Semester Grade Point Average (SGPA) ≥ 6.0 (in each Semester) and final Cumulative Grade Point Average (CGPA) (i.e., CGPA at the end of PGP) ≥ 6.0, to successfully complete the PGP.

Note: (1) The SGPA will be computed and printed on the marks memo only if the student passes in all the subjects offered and gets minimum B grade in all the subjects.

(2) CGPA is calculated only when the student passes in all the subjects offered in all the semesters.

6.4 Marks and Letter Grades obtained in all those Subjects covering the above specified 68 Credits alone shall be considered for the calculation of final CGPA, which shall be indicated in the Grade Card / Marks Memo of II Year II Semester.

6.5 If a student registers for some more 'extra Subjects' (in the parent Department or other Departments/Branches of Engineering.) other than those listed Subjects totaling to 68 Credits as specified in the Course Structure, the performances in those 'extra Subjects' (although evaluated and graded using the same procedure as that of the required 68 Credits) will not be taken into account while calculating the SGPA and CGPA. For such 'extra Subjects' registered, % marks and Letter Grade alone will be indicated in the Grade Card, as a performance measure, subject to completion of the Attendance and Academic Requirements as stated in Items 5 and 6.1 – 6.4 above.

6.6 Students who fail to earn 68 Credits as per the specified Course Structure, and as indicated above, within 4 Academic Years from the date of Commencement of their I Year, shall forfeit their seats in M.Tech. Programme and their admissions shall stand cancelled.

6.7 When a student is detained due to shortage of attendance in any subject(s)/seminar in any semester, no Grade Allotment will be done for such Subject(s)/Seminar, and SGPA/ CGPA calculations of that Semester will not include the performance evaluations of such subject(s)/seminar in which he got detained. However, he becomes eligible for re-registration of such subject(s)/seminar (in which he got detained) in the subsequent Semester(s), as and when next offered, with the Academic Regulations of the Batch into which he gets readmitted, by paying the stipulated fees per subject. In all these re-registration cases, the student shall have to secure a fresh set of Internal Marks (CIE) and End Semester Examination Marks (SEE) for performance evaluation in such subject(s), and subsequent SGPA/ CGPA calculations.

6.8 A student eligible to appear in the Semester End Examination (SEE) in any subject, but absent at it or failed (failing to secure B Grade or above), may reappear for that subject at the supplementary examination (SEE) as and when conducted. In such cases, his Internal Marks (CIE) assessed earlier for that Subject/ Course will be carried over, and added to the marks to be obtained in the supplementary examination (SEE), for evaluating his performance in that Subject.

7. EVALUATION - DISTRIBUTION AND WEIGHTAGE OF MARKS

7.1 The performance of a Student in each Semester shall be evaluated Subject-wise (irrespective of Credits assigned) with a maximum of 100 Marks for Theory or Practical's or Mini Project with Seminar or Drawing/Design etc; however, the M.Tech. Project Work (Major Project) will be evaluated by the external examiner for 100 Marks.

7.2 **a)** For Theory Subjects (inclusive of Minor Courses), during the Semester, there shall be 2 mid-term examinations for 25 marks (with duration of 120 minutes). Further, there will be an allocation of 5 marks for Assignment.

b) The first mid-term examination shall be conducted for the first 50% of the syllabus, and the second mid-term examination shall be conducted for the remaining 50% of the syllabus.

c) First Assignment should be submitted before the conduct of the first mid-term examinations, and the Second Assignment should be submitted before the conduct of the second mid-term examinations. The Assignments shall be as specified by the concerned subject teacher.

d) The first mid-term examination Marks and first Assignment Marks shall make one set of CIE Marks, and the second mid-term examination Marks and second Assignment Marks shall make second set of CIE Marks. The final CIE marks (for total of 30) are the better of these two mid-term examinations in each subject.

7.3 For Practical Subjects, there shall be a Continuous Internal Evaluation (CIE) during the Semester for 30 Internal Marks, and 70 Marks are assigned for Lab/Practical's Semester End Examination (SEE). Out of the 30 Marks for Internals, day-to-day work assessment in the laboratory shall be evaluated for 20 Marks; and the performance in an internal Lab/Practical Test shall be evaluated for 10 marks, there shall be two internal Lab/Practical Test in a semester and the better of these two shall be taken as final marks. The SEE for Lab / Practical's shall be conducted at the end of the Semester by the concerned Lab teacher and external examiner appointed by the Head of the Institution.

7.4 For mandatory (audit) courses, a student has to secure 40 marks out of 100 marks (i.e. 40% of the marks allotted) in the continuous internal evaluation for passing the subject/course. No marks or letter grades shall be allotted for mandatory (audit) courses. Only Pass/Fail shall be indicated in Grade Card.

7.5 There shall be a Mini Project with Seminar presentation in I Year II Semester for 100 marks, for which the student shall collect the information on a specialized topic, prepare a Mini Project Report and submit to the department. The Continuous Internal Evaluation (CIE) of 30 Marks evaluated by the guide / supervisor and Semester End Examination (SEE) of 70 marks evaluated by the committee. The evaluation committee consisting of Head of the Department, Mini Project Guide and senior faculty as appointed by Head of the Department.

7.6 Guidelines for Project Work Evaluation:

a) The Project shall start immediately after the completion of I year II semester. Every Student must register for his M.Tech. Project Work, within the 4 weeks after the completion of I year II Semester. The student registered for the Project work shall work for two semesters. After Registration and in consultation with the guide, the Student has to present the title, objective and plan of action of his project work to the Project Review Committee (PRC) for approval within 6 weeks after the completion of I year II Semester. Only after obtaining the approval of the PRC, the student can initiate the Project work.

b) A Project Review Committee (PRC) shall be constituted by Head of the Department and shall consist of the Head of the Department (Chairperson) Project Guide and one senior faculty member of the Department.

c) If a student wishes to change his Guide or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/Guide leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Guide or topic as the case may be.

7.7 Monitoring of Project work progress by PRC

a) The PRC will monitor the progress of the Project Work of the student. Project work Review-I will be held at the end of the III Semester (II Year I Semester) and Project work Review- II will be held at the end of the IV Semester (II year II Semester) before the submission of Project Report/ Dissertation.

b) **The Project Work Review-I:** There shall be a Dissertation-I/Industrial Project-I during the III Semester (II Year I Semester). The Dissertation-I/Industrial Project-I shall be evaluated by the project external viva-voce examination committee for 70 Marks (which will be considered as SEE). The student has to get a minimum of 40% marks (28 marks out of 70 marks) for successful completion. Project guide and PRC-I shall evaluate for 30 marks (which will be considered as CIE). The guide evaluates for 15 marks and PRC-I evaluates for rest of 15 marks. The student has to secure a minimum of 50 marks (CIE + SEE) out of 100 marks to be declared successful. If the student fails to obtain the minimum marks, the student has to reappear for the Dissertation-I/Industrial Project-I during the supplementary examinations. The student shall be permitted to register Dissertation-II/Industrial Project-II only after successful completion of Dissertation-I/Industrial Project-I.

c) **The Project Work Review-II:** There shall be a Dissertation-II/Industrial Project-II during the IV Semester (II Year II Semester). The Dissertation-II/Industrial Project-II shall be evaluated by the project external viva-voce examination committee for 70 Marks (which will be considered as SEE). The student has to get a minimum of 40% marks (28 marks out of 70 marks) for successful completion. Project guide and PRC-II shall evaluate for 30 marks (which will be considered as CIE). The guide evaluates for 15 marks and PRC-II evaluates for rest of 15 marks. The student has to secure a minimum of 50 marks (CIE + SEE) out of 100 marks to be declared successful. If the student fails to obtain the minimum marks, the student has to reappear for the Dissertation-II/Industrial Project-II during the supplementary examinations.

d) To satisfy item (c), the student has to submit a soft copy of the final consolidated report of Dissertation - I & II / Industrial Project – I & II to the Head of the Department for 'ANTIPLAGIARISM' check. The Head of the Department should carry out plagiarism check and submit the report to the Principal. The Dissertation will be accepted for submission, only if the similarity index is less than 30%. If the similarity index has more than the required percentage, the student is advised to modify accordingly and re-submit the soft copy of the Dissertation only after one month. Only after submission of a hard copy of final project report in 4 copies along with plagiarism report, the Dissertation-II / Industrial Project-II shall be evaluated by the project external viva-voce examination committee. The maximum number of re-submissions of Dissertation after plagiarism check is limited to TWO.

e) The candidate has to register for the project and work for two semesters (not less than 44 weeks including registration and approval of Project-I and Project-II). After three attempts (including regular attempt), the admission is liable to be cancelled. The college authorities are advised to make plagiarism check of every soft copy of theses before submissions.

f) The Student shall be allowed to submit his Project Dissertation, only on the successful completion of all the prescribed PG Subjects (Theory and Practical's.), Mini Project with Seminar, etc. (securing B Grade or above), and after obtaining all approvals from PRC.

g) Three copies of the Dissertation Thesis certified by the supervisor shall be submitted to the College/School/Institute, after submission of a research paper related to the Dissertation work in a reputed journal / conference. A copy of the submitted research paper shall be attached to thesis.

h) The Dissertation of the student will be evaluated by the committee along with external examiner (appointed by the Head of the Institution) based on his/her presentation followed by viva-voce examination.

i) If the report of the committee is unsatisfactory, the student shall revise and resubmit the project after ONE semester, or as per the time specified by the committee. If the resubmitted report is also unsatisfactory, then the Dissertation shall be rejected summarily. No further correspondence in this matter will be entertained, if there is no specific recommendation for resubmission by the committee.

j) If the student's oral presentation is not satisfactory, the committee may defer it and the student has to re-appear for the oral presentation before the same committee for the award of degree.

k) The Committee should submit Project External examination marks to the Head of the Institution on the day of the examination.

8. Re-Admission / Re-Registration:

8.1. **Re-Admission for Discontinued Students:** Students, who have discontinued the M.Tech. Degree Programme due to any reasons whatsoever, may be considered for 'Readmission' into the same Degree Programme (with same specialization) with the Academic Regulations of the Batch into which he gets Re-admitted, with prior permission from the concerned authorities, subject to Item 3.1.

8.2. **Re-Registration for Detained Students:** When any Student is detained in a Subject (Theory / Practical / Seminar etc.) due to shortage of attendance in any Semester, he may be permitted to re-register for the same Subject in the 'same category' (Core or Elective Group) or equivalent Subject if the same Subject is not available, as suggested by the Board of Studies of that Department, as when offered in the sub-sequent Semester(s), with the Academic Regulations of the Batch into which he seeks re-registration , with prior permission from the concerned authorities, subject to Item 3.1.

9. GRADING PROCEDURE

9.1 Marks will be awarded to indicate the performance of each student in each Theory Subject, or Practical, or Mini Project with Seminar, Project, etc., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 6 above, and a corresponding Letter Grade shall be given.

9.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	Letter Grade	Grade Points
90% and above	O (Outstanding)	10
Below 90% but not less than 80%	A^+ (Excellent)	9
Below 80% but not less than 70%	A (Very Good)	8
Below 70% but not less than 60%	B^+ (Good)	7
Below 60% but not less than 50%	B (Above Average)	6
Below 50% (< 50%)	F (Fail)	0
Absent	**Ab**	**0**

9.3 A student obtaining F Grade in any Subject shall be considered 'failed' and is be required to reappear as 'Supplementary Student' in the Semester End Examination (SEE), as and when conduct. In such cases, his Internal Marks (CIE Marks) in those Subjects will remain the same as those he obtained earlier.

9.4 If a student not appear for the examinations, 'Absent' Grade will be allocated to him for any subject and shall be considered 'failed' and will be required to reappear as 'Supplementary

Student' for the Semester End Examination (SEE), as and when conducted.

9.5 A Letter Grade does not imply any specific % of marks.

9.6 In general, a student shall not be permitted to repeat any subject / course (s) only for the sake of 'Grade Improvement' or 'SGPA/CGPA Improvement.

9.7 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course (excluding Audit non-credit Courses). Then the corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

Credit Points (CP) = Grade Point (GP) x Credits … For a Course

9.8 The Student passes the subject/course only when he gets GP ≥ 6 (B Grade or above).

9.9 The Semester Grade Point Average (SGPA) is calculated by dividing the sum of credit points (ΣCP) secured from all subjects / courses registered in a semester, by the total number of credits registered during that semester. SGPA is rounded off to **two** decimal places. SGPA is thus computed as

$$\textbf{SGPA } (S_i) = \sum (C_i \times G_i) / \sum C_i$$

Where C_i is the number of credits of the i^{th} course and G_i is the grade point scored by the student in the i^{th} course.

9.10 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student in all semesters considered for registration. The CGPA is the ratio of the total credit points secured by a student in **all** registered courses in **all** Semesters, and the total number of credits registered in **all** the semesters. CGPA is rounded off to **two** decimal places. CGPA is thus computed from the I year second semester onwards, at the end of each semester, as per the formula:

$$\textbf{CGPA} = \sum (C_i \times S_i) / \sum C_i$$

where S_i is the SGPA of the i^{th} semester and C_i is the total number of credits in that semester.

Illustration of calculation of SGPA					Illustration of calculation of CGPA			
Course /Subject	Credits	Letter Grade	Grade Points	Credit Points	Semester	Credits	SGPA	Credits x SGPA
Course 1	3	A	8	24	Sem I	18	7.00	126
Course 2	3	O	10	30	Sem II	18	6.00	108
Course 3	4	B^+	7	28	Sem III	16	6.50	104
Course 4	3	B	6	18	Sem IV	16	8.00	128
Course 5	2	A^+	9	18				
Course 6	1.5	B	6	09				
Course 7	1.5	O	10	15				
Total	18			142	Total	68		426
SGPA = 142/18 = 7.89					**CGPA** =466/68 = 6.85			

9.11 For merit ranking or comparison purposes or any other listing, **only** the '**rounded off**' values of the CGPAs will be used.

9.12 For calculations listed in item 9.7 to 9.11, performance in failed subjects/courses (securing '**F**' grade) will also be taken into account, and the credits of such subjects/courses will also be included in the multiplications and summations.

10. DECLARATION OF RESULTS

10.1 Computation of SGPA and CGPA are done using the procedure in item Nos. 9.6 to 9.9.

10.2 For final percentage of marks equivalent to the computed final CGPA, the following formula may be used:

Percentage of Marks = (final CGPA – 0.5) x 10

11 AWARD OF DEGREE

11.1 After a student has satisfied the requirement prescribed for the completion of the Program and is eligible for the award of M.Tech. Degree he shall be placed in one of the following four classes based on CGPA:

Class Awarded	CGPA	Remarks
First Class with Distinction	≥ 7.75	From the aggregate marks secured from 68 credits for regular students
First Class	6.75≤ CGPA < 7.75	
Second Class	6.00≤ CGPA < 6.75	

A student with final CGPA (at the end of the **PGP) < 6.00** shall not be eligible for the Award of Degree.

11.2 First Class with Distinction will be awarded to those students who clear all the subjects in single attempt during his/her regular course of study by fulfilling the following conditions:

11.2.1 Should have passed all the subjects/courses in '**first appearance'** within the first 2 academic years (or 4 sequential semesters) for M.Tech.

11.2.2 Should have secured a CGPA ≥7.75, at the end of each of the 4 sequential semesters.

11.2.3 Should not have been detained or prevented from writing the Semester End Examinations in any semester due to shortage of attendance or any other reason, shall be placed in '**First Class with Distinction'**.

11.3 Award of Medals: Students fulfilling the conditions listed under item 11.2 alone will be eligible for award of **'College ranks'** and **'Medals'**.

11.4 Transcripts: After successful completion of prerequisite credits for the award of degree a transcript containing performance of all academic years will be issued as a final record. Duplicate transcripts will also be issued if required after the payment of requisite fee and also as per norms in vogue.

12 WITH HOLDING OF RESULTS

If the student has not paid the fee to college at any stage, or has dues pending against his/her name due to any reason what so ever, or if any case of indiscipline is pending against him/her, the result of the student may be withheld, and he/she will not be allowed to go into the next higher semester. The award or issue of the degree may also be withheld in such cases.

13 SUPPLEMENTARY EXAMINATIONS

Supplementary examinations for odd semester subject(s) / course (s) shall be conducted along with even semester regular examinations and vice versa.

14. TRANSITORY REGULATIONS

A Student - who has discontinued for any reason, or who has been detained for want of attendance as specified, or who has failed after having undergone PGP, may be considered

eligible for readmission to the same PGP with same set of Subjects/ Courses (or equivalent Subjects/ Courses as the case may be), and same Professional Electives (or from same set/category of Electives or equivalents as suggested), as and when they are offered (within the time-frame of 4 years from the Date of Commencement of his I Year I Semester).

15. STUDENT TRANSFERS

There shall be no transfers from other colleges/streams.

16 RULES OF DISCIPLINE

16.1 Any attempt by any student to influence the teachers, Examiners, faculty and staff of controller of Examination for undue favours in the exams, and bribing them either for marks or attendance will be treated as malpractice cases and the student can be debarred from the college.

16.2 When the student absents himself, he is treated as to have appeared and obtained zero marks in that subject(s) and grading is done accordingly.

16.3 When the performance of the student in any subject(s) is cancelled as a punishment for indiscipline, he is awarded zero marks in that subject(s).

16.4 When the student's answer book is confiscated for any kind of attempted or suspected malpractice the decision of the Examiner is final.

17. MALPRACTICE

17.1 **Malpractice Prevention Committee:** The committee shall examine the student's malpractice and indiscipline cases occurred, while conducting the examinations and recommend appropriate punishment to the Academic Council after taking explanation from the student and concerned invigilator as per the malpractice rules mentioned below. The committee consists of

a) Controller of Examinations - Chairman
b) Addl. Controller of Examinations.- Convener
c) Subject Expert - Member
d) Head of the Department of which the student belongs to - Member
e) The Invigilator concerned - Member

17.2 **Malpractice Rules:** Disciplinary action for improper conduct in examinations

S. No.	Nature of Malpractices / Improper Conduct	Punishment
1(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.

1(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the Principal.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6	Refuses to obey the orders of the Addl. Controller of examinations / any officer on duty or misbehaves or	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that

	creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the addl. Controller of examinations or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the addl. Controller of examinations, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not

		belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the principal for further action to award suitable punishment.	

18. SCOPE

i) The academic regulations should be read as a whole, for the purpose of any interpretation.

ii) The above mentioned rules and regulations are applicable in general to M.Tech., unless and otherwise specific.

iii) In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman of the Academic Council is final.

19. REVISION AND AMENDMENTS TO REGULATIONS

The Academic Council may revise or amend the academic regulations, course structure or syllabi at any time, and the changes or amendments made shall be applicable to all students with effect from the dates notified by the Academic Council Authorities.

———

COURSE STRUCTURE

M.Tech. (VLSI) – R20 COURSE STRUCTURE

(Applicable from the batch admitted during 2020-21 and onwards)

I – Semester									
S. No	Course Code	Subject	Hours Per Week			Credits	Scheme of Evaluation		
							Maximum Marks		
			L	T	P		Int.	Ext.	Tot.
1	20VLPC101	Digital Design and Verification	3	0	0	3	30	70	100
2	20VLPC102	Internet of Things	3	0	0	3	30	70	100
3	**Professional Elective-1**		3	0	0	3	30	70	100
	20VLPE101	CMOS Mixed Signal Circuit Design							
	20VLPE102	Digital System Design							
	20VLPE103	VLSI Signal Processing							
4	**Professional Elective-2**		3	0	0	3	30	70	100
	20VLPE104	Modeling and Synthesis with Verilog HDL							
	20VLPE105	CPLD and FPGA Architectures and Applications							
	20VLPE106	CAD of Digital System							
5	20VLPC103	Digital Design and Verification Lab	0	0	4	2	30	70	100
6	20VLPC104	Internet of Things Lab	0	0	4	2	30	70	100
7	20MC101	Research Methodology and IPR	2	0	0	2	30	70	100
8	**Audit Course -1**		2	0	0	0	100	-	100
	20AC101	English for Research Paper Writing							
	20AC102	Value Education							
	20AC103	Constitution of India							
TOTAL			**16**	**0**	**8**	**18**	**310**	**490**	**800**

II – Semester (I – Year)									
S. No.	Course Code	Subject	Hours Per Week			Credits	Scheme of Evaluation		
							Maximum Marks		
			L	T	P		Int.	Ext.	Tot.
1	20VLPC201	Analog and Digital CMOS VLSI Design	3	0	0	3	30	70	100
2	20VLPC202	VLSI Design Verification and Testing	3	0	0	3	30	70	100
3	**Professional Elective -3**		3	0	0	3	30	70	100
	20VLPE201	Memory Technologies							
	20VLPE202	SOC Design							
	20VLPE203	Low power VLSI Design							
4	**Professional Elective -4**		3	0	0	3	30	70	100
	20VLPE204	Functional Verification using Hardware Verification Languages							
	20VLPE205	MOS Device Modeling and Characterization							
	20VLPE206	Physical Design Automation							
5	20VLPC203	Analog and Digital CMOS VLSI Design Lab	0	0	4	2	30	70	100
6	20VLPC204	VLSI Design Verification and Testing Lab	0	0	4	2	30	70	100
7	20VLPR201	Mini Project with Seminar	0	0	4	2	30	70	100
8	**Audit Course -2**		2	0	0	0	100	-	100
	20AC201	Pedagogy Studies							
	20AC202	Stress Management by Yoga							
	20AC203	Personality Development through Life Enlightenment Skills							
TOTAL			**14**	**0**	**12**	**18**	**310**	**490**	**800**

III – Semester									
S. No	Course Code	Subject	Hours Per Week			Credits	Scheme of Evaluation		
							Maximum Marks		
			L	T	P		Int.	Ext.	Tot.
1	**Professional Elective -5**		3	0	0	3	30	70	100
	20VLPE301	Microchip Fabrication Techniques							
	20VLPE302	Design for Testability							
	20VLPE303	Nano materials and Nanotechnology							
2	**Open Elective**		3	0	0	3	30	70	100
	20MEOE301	Composite Materials							
	20CEOE302	Construction Management							
	20ECOE303	VLSI Design							
	20CSOE304	Data Mining and Analytics							
3	20VLPR301	Project – I / Dissertation Phase -I	0	0	20	10	30	70	100
TOTAL			**6**	**0**	**20**	**16**	**90**	**210**	**300**

IV – Semester									
S. No.	Course Code	Subject	Hours Per Week			Credits	Scheme of Evaluation		
							Maximum Marks		
			L	T	P		Int.	Ext.	Tot.
1	20VLPR401	Project – II / Dissertation Phase -II	0	0	32	16	30	70	100
TOTAL			**0**	**0**	**32**	**16**	**30**	**70**	**100**

Total Credit for the Programme PG Credits: = 18+ 18+16+16 = 68

I-M.TECH.-I-SEMESTER SYLLABUS

DIGITAL DESIGN AND VERIFICATION

I-M.Tech.-I-Sem.	L	T	P	C
Course Code: 20VLPC101	3	0	0	3

Course Outcomes: Upon completion of the course, the student will be able to

1. explain the basic concepts of digital systems
2. outline the fundamentals of HDL & Verilog
3. analyze System Verilog and Verification
4. examine Current challenges in physical design
5. design the Programmable Logic Devices

UNIT-I

Revision of basic Digital systems: Combinational Circuits, Sequential Circuits, Logic families Synchronous FSM and asynchronous design, Meta stability, Clock distribution and issues, basic building blocks like PWM module, pre-fetch unit, programmable counter, FIFO, Booth's multiplier, ALU, Barrel shifter etc.

UNIT-II

Verilog/VHDL Comparisons and Guidelines, Verilog: HDL fundamentals, simulation, and test-bench design, Examples of Verilog codes for combinational and sequential logic, Verilog AMS

UNIT-III

System Verilog and Verification: Verification guidelines, Data types, procedural statements and routines, connecting the test bench and design, Assertions, Basic OOP concepts, Randomization, Introduction to basic scripting language: Perl, Tcl/Tk

UNIT-IV

Current challenges in physical design: Roots of challenges, Delays: Wire load models Generic PD flow, Challenges in PD flow at different steps, SI Challenge - Noise & Crosstalk, IR Drop, Process effects: Process Antenna Effect & Electromigration.

UNIT-V

Programmable Logic Devices: Introduction, Evolution: PROM, PLA, PAL, Architecture of PAL's, Applications, Programming PLD's, FPGA with technology: Anti-fuse, SRAM, EPROM, MUX,FPGA structures, and ASIC Design Flows, Programmable Interconnections, Coarse grained reconfigurable devices

Text Books:

1. Douglas Smith, “HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs Using VHDL or Verilog”, Doonepublications,1998.
2. Samir Palnitkar, “Verilog HDL: A guide to Digital Design and Synthesis”, Prentice Hall, 2nd Edition,2003.

References:

1. Doug Amos, Austin Lesea, Rene Richter, “FPGA based Prototyping Methodology Manual”, Synopsys Press,2011.
2. Christophe Bobda, “Introduction to Reconfigurable Computing, Architectures, Algorithms and Applications”, Springer,2007.
3. Janick Bergeron, “Writing Test benches: Functional Verification of HDL Models”, Second Edition, Springer,2003.

INTERNET OF THINGS

I-M.Tech.-I-Sem. **L T P C**
Course Code: 20VLPC102 **3 0 0 3**

Course Outcomes: Upon completion of the course, the student will be able to

1. explain the basic concept of internet of things and characteristics.
2. describe the m2m with necessary protocols
3. discuss about python scripting language
4. make use of web based services on IOT devices
5. examine the different type of case study & advanced IOT applications

UNIT -I

Introduction to Internet of Things: Definition and Characteristics of IoT, Physical Design of IoT – IoT Protocols, IoT communication models, IoT Communication APIs IoT enabled Technologies – Wireless Sensor Networks, Cloud Computing, Communication protocols, Embedded Systems, IoT Levels and Templates.

UNIT -II

IoT Architecture: History of IoT, M2M – Machine to Machine, Web of Things, IoT protocols Applications: Remote Monitoring & Sensing, Controlling, Performance Analysis The Architecture The Layering concepts , IoT Communication Pattern, IoT protocol Architecture, The 6LoWPAN Security aspects in IoT.

UNIT - III

Introduction to Python: Language features of Python, Data types, data structures, Control of flow, functions, modules, packaging, file handling, data/time operations, classes, Exception handling Python packages. IoT Physical Devices and Endpoints– Introduction to Raspberry PI-Interfaces (serial, SPI, I2C) Programming – Python program with Raspberry PI with focus of interfacing external gadgets, controlling output, reading input from pins.

Unit-IV

IoT Application Development: Application Protocols MQTT, REST/HTTP, COAP, IoT Physical Servers and Cloud Offerings– Introduction to Cloud Storage models and communication APIs Webserver – Web server for IoT, Cloud for IoT, Python web application framework Designing a REST ful web API.

UNIT V

Case Study & advanced IoT Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi /Arduino).

Text Books:

1. Internet of Things - A Hands-on Approach, Arshdeep Bahga and Vijay Madisetti, Universities Press, 2015, ISBN: 9788173719547.
2. Getting Started with Raspberry Pi, Matt Richardson & Shawn Wallace, O'Reilly (SPD), 2014, ISBN: 9789350239759.

References:

1. Internet of Things (A Hands-on-Approach) , Vijay Madisetti , Arshdeep Bahga.
2. Designing the Internet of Things , Adrian McEwen (Author), Hakim Cassimally.

CMOS MIXED SIGNAL CIRCUIT DESIGN
(Professional Elective – 1)

I-M.Tech.-I-Sem.	L	T	P	C
Course Code: 20VLPE101	3	0	0	3

Course Outcomes: Upon completion of the course, the student will be able to

1. analyze the switched capacitor circuits
2. illustrate the working and applications of phased lock loop
3. outline the fundamentals of data converter
4. apply the concepts of nyquist rate A/D converters
5. explain the oversampling converters

UNIT – I

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, bi-quad filters.

UNIT – II

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge Pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT – III

Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT – IV

Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time interleaved converters.

UNIT – V

Oversampling Converters: Noise shaping modulators, Decimating filters an interpolating filters, Higher order modulators, Delta sigma modulators with multi-bit quantizers, Delta sigma D/A

Text Books:

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, TMH Edition, 2002
2. Philip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. David A. Johns,Ken Martin, “Analog Integrated Circuit Design”, Wiley Student Edition, 2013

References:

1. Rudy Van De Plassche, “CMOS Integrated Analog-to- Digital and Digital-to-Analog converters”, Kluwer Academic Publishers.
2. Richard Schreier, “Understanding Delta-Sigma Data converters”, Wiley Interscience.
3. R. Jacob Baker, “CMOS Mixed-Signal Circuit Design”, Wiley Interscience.

DIGITAL SYSTEM DESIGN
(Professional Elective – 1)

I-M.Tech.-I-Sem. **L T P C**
Course Code: 20VLPE102 **3 0 0 3**

Course Outcomes: Upon completion of the course, the students will be able to
1. explain the basic concept mapping algorithms into architectures
2. summarize the combinational network delay
3. outline the sequencing static circuits
4. discuss the data path and array subsystems
5. illustrate the reconfigurable computing.

UNIT–I

Mapping Algorithms into Architectures: Data path synthesis, control structures, critical path and Worst case timing analysis. FSM and Hazards

UNIT–II

Combinational Network Delay: Power and energy optimization in combinational logic circuit. Sequential machine design styles. Rules for clocking. Performance analysis

UNIT–III

Sequencing Static Circuits: Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.

.

UNIT–IV

Data path and Array Subsystems: Addition / Subtraction, Comparators, counters, coding, Multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory

UNIT–V

Reconfigurable Computing : Fine grain and Coarse grain architectures, Configuration architectures Single context, Multi context, partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing.

Text Books:

1. N.H.E.Weste, D. Harris, “CMOS VLSI Design (4th edition)”, Pearson, 2010.
2. W.Wolf, “FPGA- based System Design”, Pearson, 2004.
3. S.Hauck&A.DeHon, “Reconfigurable computing: the theory and practice of FPGA-based computation”, Elsevier, 2008.

References:

1. F.P. Prosser & D. E. Winkel, “Art of Digital Design”, 1987.
2. R.F.Tinde, “Engineering Digital Design”, (2nd edition), Academic Press, 2000.
3. C. Bobda, “Introduction to reconfigurable computing”, Springer, 2007.
4. M.Gokhale&P.S.Graham, “Reconfigurable computing: accelerating computation with field-programmable gate arrays”, Springer, 2005.
5. C.Roth,” Fundamentals of Digital Logic Design”, Jaico Publishers, 5th edition., 2009.
6. Recent literature in Digital System Design.

VLSI SIGNAL PROCESSING
(Program Elective – 1)

I-M.Tech.-I-Sem. **L T P C**
Course Code: 20VLPE103 **3 0 0 3**

Course Outcomes: Upon completion of the course, the students will be able to

1. discuss the basic concept DSP
2. distinguish folding and unfolding
3. illustrate the systolic architecture design
4. determine the fast convolution
5. discuss the low power design

UNIT – I
Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms. Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power. Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques.

UNIT – II
Folding and Unfolding: Folding: Introduction -Folding Transform – Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding.

UNIT – III
Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays.

UNIT – IV
Fast Convolution: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection.

UNIT – V
Low Power Design: Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches. Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

Text Books:
1. Keshab K. Parthi, “VLSI Digital Signal Processing- System Design and Implementation”, 1998, Wiley Inter Science.
2. Kung S. Y, H. J. While House, T. Kailath, “VLSI and Modern Signal processing”, 1985, Prentice Hall.

References:
1. Jose E. France, Yannis Tsividis, “Design of Analog – Digital VLSI Circuits for Tele-communications and Signal Processing”, 1994, Prentice Hall.
2. Medisetti V. K, “VLSI Digital Signal Processing”, 1995, IEEE Press (NY), USA.

MODELING AND SYNTHESIS WITH VERILOG HDL
(Professional Elective – 2)

	L	T	P	C
I-M.Tech.-I-Sem.				
Course Code: 20VLPE104	**3**	**0**	**0**	**3**

Course Outcomes: Upon completion of the course, the students will be able to

1. explain the basic concept of verilog hardware description languages (HDL)
2. outline the dataflow modeling of digital circuits
3. make use of behavioral level of digital circuits
4. design combinational circuits
5. construct sequential circuits

UNIT– I

Basics of Verilog HDL: Lexical conventions, data types, system tasks and compiler directives. Units and Ports: Units, ports, hierarchical names. Gate-Level Modeling: Gate types, gate delays.

UNIT – II

Dataflow Modeling: Continuous assignments, delays, expressions, operators, and operands, operator types, examples.

UNIT – III

Behavioral Modeling: Structured procedures, procedural assignments, timing controls, conditional statements, multiway branching, loops, sequential and parallel blocks, generate blocks, examples.

UNIT – IV

Combinational System Design: Documentation standards, Circuit timings, Adders, Subtractors, Exclusive OR gates, Decoders, Encoders, Multiplexers, Comparators,

UNIT -V

Sequential System Design: Design of Latches and flip flops-SR, JK, D, T. Design of Shift Registers, BCD Counter, Ripple Counter, Mod-8 Counter

Text Books:

1. Samir Palnitkar, Verilog HDL, 2/e, Pearson Education, 2013.
2. Charles Roth, Digital Systems Design using Verilog, Cengage Learning, 2014
3. J. Bhasker, Verilog Synthesis Primer, B. S. Publications, 2011

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS
(Professional Elective –2)

I-M.Tech.-I-Sem. **L T P C**
Course Code: 20VLPE105 **3 0 0 3**

Course Outcomes: Upon completion of the course, the students will be able to

1. explain the concept of programmable logic devices
2. outline the field programmable gate arrays
3. make use of SRAM programmable FPGAs
4. make use of anti-fuse programmed FPGAs
5. illustrate the design applications

UNIT – I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices–Read Only Memories, Programmable Logic Arrays,Programmable Array Logic,Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation

UNIT – II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures,Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT – III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures

UNIT – IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture,The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT – V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books:

1. Stephen M. Trimberger, “Field Programmable Gate Array Technology”, Springer International Edition.
2. Charles H. Roth Jr, Lizy Kurian John, “Digital Systems Design”, Cengage Learning.

References:

1. John V. Oldfield, Richard C. Dorf, “Field Programmable Gate Arrays”, Wiley India.
2. Pak K. Chan/Samiha Mourad, “Digital Design Using Field Programmable Gate Arrays”, Pearson Low Price Edition.
3. Ian Grout, “Digital Systems Design with FPGAs and CPLDs”, Elsevier, Newnes.
4. Wayne Wolf, “FPGA based System Design”, Prentice Hall Modern Semiconductor Design Series.

CAD OF DIGITAL SYSTEM
(Professional Elective –2)

	L	T	P	C
I-M.Tech.-I-Sem.				
Course Code: 20VLPE106	**3**	**0**	**0**	**3**

Course Outcomes: Upon completion of the course, the students will be able to

1. explain the concept of VLSI methodologies
2. explore the VLSI design automation tools
3. make use of general purpose methods
4. discuss logic & high level synthesis and verification
5. summarize the physical design automation of FPGA and MCM

UNIT -I

Introduction to VLSI Methodologies: Design and Fabrication of VLSI Devices, Fabrication,Process and its impact on Design.

UNIT-II

VLSI Design Automation Tools: Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

UNIT-III

General Purpose Methods: General purpose methods for combinational optimization – partitioning, floor planning and pin assignment placement and routing.

UNIT –IV

Logic & High Level Synthesis and Verification: Binary-decision Diagrams, Two-level Logic Synthesis, High-level Synthesis , Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling , High-level Transformations

UNIT –V

Physical Design Automation of FPGA and MCM: FPGA Technologies, Physical Design Cycle for FPGAs: Partitioning, Routing, MCM Technologies: MCM Physical Design Cycle, Partitioning, Placement, Routing

References:

1. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”.
2. S.H. Gerez, “Algorithms for VLSI Design Automation

DIGITAL DESIGN AND VERIFICATION LAB

	L	T	P	C
I-M.Tech.-I-Sem.				
Course Code: 20VLPC103	**0**	**0**	**4**	**2**

Course Outcomes: Upon completion of the course, the students will be able to

1. test logic gates
2. design combinational circuits
3. develop sequential circuits
4. analyze finite state machines
5. construct CMOS circuit schematics and their layouts

List of Experiments *(*Any six experiments from each part are to be conducted):
Design and implementation of the following CMOS digital/analog circuits using Cadence /Mentor Graphics / Synopsys /Equivalent CAD tools:

Part -A

1. Basic All logic gates
2. 8:1 Mux/Demux
3. 3 model styles Full Adder
4. 3 to 8 Decoder
8 to 3 Encoder Priority (without & with)
4 bits Binary to gray code converters
5. 2-bit Magnitude comparator
6. D, SR and JK Flip flops.
7. Single and Dual port SRAM
8. Sequence Detector using Mealy and Moore type state machines.
9 Bit Parallel Adder using four bit tasks and functions.
9. D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters.
10. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.

Part -B

Transistor Level implementation of CMOS circuits

11. CMOS Inverter/ Buffer
12. CMOS NAND / NOR gates.
13. CMOS XOR
14. CMOS AND/OR gates
15. 28T Full Adder
16. 4:1 Multiplexer
17. Latch
18. Combinational circuits
19. Pass transistor
20. Complex circuits
21. 2:4 Decoder

References:

1. Digital Design and Verification Lab - Manual, Department of ECE , CMRIT, Hyd.

INTERNET OF THINGS LAB

I-M.Tech.-I-Sem. **L T P C**
Course Code: 20VLPC104 **0 0 4 2**

Course Outcomes: Upon completion of the course, the student will be able to

1. improve working on basic IoT devices
2. determine learning and utilization of IoT devices
3. develop automation work-flow in IoT enabled environment
4. recommend working on advance IoT Systems
5. take part in practicing and monitoring remotely

List of Experiments (Minimum **10** experiments to be conducted**)**

1. Start Raspberry Pi and various Linux commands in command terminal window: ls, cd, touch, mv, rm, man, mkdir, rmdir, tar, gzip, cat, more, less, ps, sudo, cron, chown, chgrp, ping etc.
2. Python programs on Pi like: Read your name and print Hello message with name Read two numbers and print their sum, difference, product and division. Word and character count of a given string Area of a given shape (rectangle, triangle and circle) reading shape and appropriate values from standard input Print a name ‘n’ times, where name and n are read from standard input, using for and while loops. Handle Divided by Zero Exception. Print current time for 10 times with an interval of 10 seconds .Read a file line by line and print the word count of each line.
3. Write a program on Light an LED.
4. Write a program on input from two switches and switch on corresponding LEDs
5. Write a program on Flash an LED at a given on time and off time cycle, where the two times are taken from a file.
6. Write a program on Flash an LED based on cron output (acts as an alarm)
7. Write a program on Switch on a relay at a given time using cron, where the relay’s contact terminals are connected to a load.
8. Write a program on Access an image through a Pi web cam.
9. Write a program on Control a light source using web page.
10. To interface Bluetooth with Raspberry Pi and write a program to send sensor data to smart phone using Bluetooth.
11. Write a program on Raspberry Pi to publish temperature data to MQTT broker.
12. Write a program on Raspberry Pi to subscribe to MQTT broker for temperature data and print it.

References:

1. Internet of Things Lab Manual, Department of ECE, CMRIT, Hyd.

RESEARCH METHODOLOGY AND IPR

	L	T	P	C
I-M.Tech.-I-Sem.				
Course Code: 20MC101	**2**	**0**	**0**	**2**

Course Outcomes: At the end of this course, students will be able to

1. formulate research problem
2. analyze research related information
3. follow research ethics
4. perceive nature of IPR and its development
5. Outline the patent rights

UNIT –I:
Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT - II:
Effective literature studies approaches, analysis Plagiarism, Research ethics.

UNIT - III:
Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT - IV:
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT - V:
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.
New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

References:

1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science& engineering students’”
2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”
3. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners”
4. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007.
5. Mayall , “Industrial Design”, McGraw Hill, 1992.
6. Niebel , “Product Design”, McGraw Hill, 1974.
7. Asimov , “Introduction to Design”, Prentice Hall, 1962.
8. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “ Intellectual Property in New Technological Age”, 2016.

ENGLISH FOR RESEARCH PAPER WRITING
(AUDIT COURSE - 1)

I-M.Tech.-I-Sem. **L T P C**
Course Code: 20AC101 **2 0 0 0**

OUTCOME: Upon completion of the course, the students will be able to

1. determine that how to improve your writing skills and level of readability
2. Learn about what to write in each section
3. determine the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

UNIT- I

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT- II

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT- III

Review of the Literature, Methods, Results, Discussion, Conclusions, Final Check.

UNIT- IV

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature

UNIT- V

Skills are needed when writing the methods, skills needed when writing the Results, skills are needed when writing the Discussion, and skills are needed when writing the Conclusions

UNIT- VI

Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

Reference:

1. Goldbort R Writing for Science, Yale University Press (available on Google Books)
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

VALUE EDUCATION
(AUDIT COURSE - 1)

I-M.Tech.-I-Sem.	L	T	P	C
Course Code: 20AC102	2	0	0	0

OUTCOME: Upon completion of the course, the students will be able to

1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

UNIT- I

Values and self-development –Social values and individual attitudes, Work ethics, Indian vision of humanism., Moral and non- moral valuation. Standards and principles, Value judgements

UNIT- II

Importance of cultivation of values, Sense of duty. Devotion, Self-reliance. Confidence, Concentration, Truthfulness, Cleanliness, Honesty, Humanity. Power of faith, National Unity,Patriotism.Love for nature ,Discipline

UNIT- III

Personality and Behavior Development - Soul and Scientific attitude, Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness, Avoid fault Thinking, Free from anger, Dignity of labour, Universal brotherhood and religious tolerance, True friendship, Happiness Vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, Doing best for saving nature

UNIT- IV

Character and Competence –Holy books vs Blind faith, Self-management and Good health, Science of reincarnation, Equality, Nonviolence ,Humility, Role of Women, All religions and same message, Mind your Mind, Self-control, Honesty, Studying effectively.

REFERENCE:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

CONSTITUTION OF INDIA
(AUDIT COURSE - 1)

	L	T	P	C
I-M.Tech.-I-Sem.				
Course Code: 20AC103	**2**	**0**	**0**	**0**

OUTCOME: Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.

UNIT- I

History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working), Preamble Salient Features

UNIT- II

Contours of Constitutional Rights & Duties: Fundamental Rights, Right to Equality, Right to Freedom,Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy ,Fundamental Duties.

UNIT- III

Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions

UNIT-IV

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation, Pachayat Raj: Introduction, PRI: Zilla Pachayat., lected officials and their roles, CEO Zilla Pachayat: Position and role., Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy

UNIT- V

Election Commission: Election Commission: Role and Functioning., Chief Election Commissioner and Election Commissioners, State Election Commission: Role and Functioning, Institute and Bodies for the welfare of SC/ST/OBC and women.

REFERENCE:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

I-M.TECH.-II-SEMESTER SYLLABUS

ANALOG AND DIGITAL CMOS VLSI DESIGN

I-M.Tech.-II-Sem. **L T P C**
Course Code: 20VLPC201 **3 0 0 3**

Course Outcomes: Upon completion of the course, the students will be able to

1. explain the basics of MOS structure
2. make use of the physical design flow
3. analyze the sequential logic and non-bistable sequential circuit
4. discuss the single stage amplifier
5. Design different types of multistage amplifiers

UNIT- I

Review of MOS Structure: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

UNIT- II

Physical Design Flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

UNIT- III

Sequential Logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers.
Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

UNIT- IV

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT- V

Passive and Active Current Mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise
Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

References:

1. J P Rabaey, A P Chandrakasan, B Nikolic, “Digital Integrated circuits: A design perspective”, Prentice Hall electronics and VLSI series, 2ndEdition.
2. Baker, Li, Boyce, “CMOS Circuit Design, Layout, and Simulation”, Wiley, 2ndEdition.
3. BehzadRazavi , “Design of Analog CMOS Integrated Circuits”, TMH,2007.
4. Phillip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford, 3rd Edition.
5. R J Baker, “CMOS circuit Design, Layout and Simulation”, IEEE Inc.,2008.
6. Kang, S. and Leblebici, Y., “CMOS Digital Integrated Circuits, Analysis and Design”, TMH,3rdEdition.
7. Pucknell, D.A. and Eshraghian, K., “Basic VLSI Design”, PHI, 3rdEdition.

VLSI DESIGN VERIFICATION AND TESTING

I-M.Tech.-II-Sem.	L	T	P	C
Course Code: 20VLPC202	3	0	0	3

Course Outcomes: Upon completion of the course, the students will be able to

1. explain the basic concepts of verification guidelines
2. explore the various data types
3. discuss the procedural statements and routines
4. analyze the system verilog assertions
5. make use the randomization

UNIT-I

Verification guidelines: Verification Process, Basic Test bench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Test bench components, Layered test bench, Building layered test bench, Simulation environment phases, Maximum code reuse, Test bench performance.

UNIT-II

Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typedef , Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.

UNIT -III

Procedural statements and routines: Procedural statements, tasks, functions and void functions, Routine arguments, Returning from a routine, Local data storage, Time values Connecting the test bench and design: Separating the test bench and design.
Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.

UNIT-IV

SystemVerilog Assertions: Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a test bench.

UNIT -V

Randomization: Introduction, What to randomize, Randomization in SystemVerilog, Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre-randomize and post randomize functions,

Text Books:

1. Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers
3. IEEE1800-2009standard(IEEE Standard for System Verilog Unified Hardware Design, Specification and Verification Language).

References:

1. System Verilog website –www.systemverilog.org
2. http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilogEvents.pdf
3. General reuse information and resourceswww.design-reuse.com
4. OVM, UVM(on top of SV)www.verificationacademy.com
5. VerificationIPresourceshttp://www.cadence.com/products/fv/verification_ip/pages/default.aspx

MEMORY TECHNOLOGIES
(Professional Elective – 3)

	L	T	P	C
I-M.Tech.-II-Sem.				
Course Code: 20VLPE201	**3**	**0**	**0**	**3**

Course Outcomes: Upon completion of the course, the students will be able to

1. explain the basic concepts of random access memory technologies
2. discuss about volatile memories
3. outline the concepts of non-volatile memories
4. describe the semiconductor memory reliability and radiation effects
5. illustrate the advanced memory technologies and high-density memory packing technologies

UNIT-I:
Random Access Memory Technologies: Static Random Access Memories (SRAMs),SRAM Cell Structures ,MOS SRAM Architecture ,MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT-II
Volatile Memories: DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

UNIT-III
Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell ,OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT-IV
Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Non-volatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

UNIT-V
Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

References:
1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Inter science
2. KiyooItoh, “VLSI memory chip design”, Springer International Edition
3. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability ,PHI

SOC DESIGN
(Professional Elective – 3)

I-M.Tech.-II-Sem.	L	T	P	C
Course Code: 20VLPE202	3	0	0	3

Course Outcomes: Upon completion of the course, the students will be able to

1. Explain basic concept of ASIC
2. Discuss about NISC
3. Illustrate the basic concepts Simulation
4. Describe Low power SoC design
5. Make use of Synthesis

UNIT-I

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP)concepts.

UNIT-II

NISC: Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT-III

Simulation: Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems. SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Unit -IV

Low power SOC design / Digital system: Overview of Low power SoC design / Digital system, Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Unit-V

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints. Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

Text Books:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press,2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET,2006
3. Rochit Rajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000
4. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann,2008
5. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011

LOW POWER VLSI DESIGN
(Professional Elective – 3)

	L	T	P	C
I-M.Tech.-II-Sem.				
Course CodE: 20VLPE203	**3**	**0**	**0**	**3**

Course Outcomes: Upon completion of the course, the students will be able to

1. Identify the sources of power dissipation in digital IC systems.
2. Discuss the Low Power Circuit Techniques.
3. Examine the different techniques of low power clock distribution.
4. Describe about leakage sources and reduction techniques.
5. compare different types of memories and processors.

UNIT-I

Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

UNIT-II

Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

UNIT-III

Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network. Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

UNIT-IV

Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

UNIT-V

Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits

Text Books:

1. P. Rashinkar, Paterson and L. Singh, “Low Power Design Methodologies”, Kluwer Academic , 2002
2. Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons Inc.,2000.
3. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley,1999.
4. A.P.Chandrasekaran ,R.W.Broadersen,“Lowpower digital CMOS design”, Kluwer,1995
5. Gary Yeap, “Practical low power digital VLSI design”, Kluwer,1998.

FUNCTIONAL VERIFICATION USING HARDWARE VERIFICATION LANGUAGES
(Professional Elective – 4)

I-M.Tech.-II-Sem.	**L**	**T**	**P**	**C**
Course Code: 20VLPE204	**3**	**0**	**0**	**3**

Course Outcomes: Upon completion of the course, the students will be able to

1. Discuss basics of System Verilog tasks & functions
2. Describe the Test Bench for System Verilog
3. Explain the basic concepts of Assertions
4. Illustrate the operators and simulation methodology for SVA
5. Classify the verification languages and implementation standards

UNIT -I
System Verilog Tasks & Functions:
Data Types, Arrays, Structures, Unions, Procedural Blocks, Tasks & Functions, Procedural Statements, Interfaces, Basic OOPs, Randomization, Threads & Inter Process Communication, Advanced OOPs &Test bench guidelines, Advanced Interfaces.

UNIT -II
System Verilog Test Bench:
A Complete System Verilog Test Bench (SVTB), Functional Coverage in System Verilog, Interfacing with C, FSM Modeling with SV, Connecting Test bench & Design, Behavioral& Transaction Level Modeling with SV

UNIT -III
System Verilog Assertions:
Introduction to SVA, Building blocks, Properties, Boolean expressions, Sequence, Single & Multiple Clock definitions, Implication operators (Overlapping & Non-overlapping), Repetition operators, Built-in System functions ($past, $stable, $onehot, $onehot0, $isunknown).Constructs (ended, and, intersect, or, first-match, throughout, within, disableiff, expect, matched, if –else), assertion directives, nested implication, formal arguments in property.

UNIT -IV
Operators and Simulation Methodology:
SVA using local variables, calling subroutines, SVA for functional coverage, Connecting SVA to the Design or Test bench, SVA for FSMs, Memories, Protocol checkers, SVA Simulation Methodology, **Assertions:** Practice & Methodology, Re-use of Assertions, Tracking coverage with Assertions, Using SVA with other languages.

UNIT -V
Functional Verification coverage using design,verification languages and implementation standards:
Verilog IEEE 1364,VHDL IEEE 1076,System Verilog IEEE 1800, Property Specific Language(PSL) IEEE 1850, System C™ IEEE 1666, Encryption IEEE 1735, e Verification Language IEEE1647, Open Verification Methodology (OVM) and Universal Verification Methodology(UVM).

Text Books:

1. System Verilog for design: a guide to using System Verilog for hardware design and modeling By Stuart Sutherland, Simon Davidmann, Peter Flake Edition: illustrated Published by Springer, 2004 ISBN 1402075308, 9781402075308
2. System Verilog for Verification: A Guide to Learning the Test bench Language Features By Chris Spear Edition: 2, Published by Springer, 2008 ISBN 0387765298, 9780387765297
3. A Practical guide for System Verilog Assertions By Srikanth Vijayaraghavan & Meyyappan Ramanathan Edition: illustrated Published by Springer, 2005 ISBN 0387260498, 9780387260495
4. The Art of Verification with System Verilog Assertions By Faisal I.Haque, Jonathan Michelson,KhizarA.Khan Published by Verification Central 2006 ISBN-13:978-0-9711994- 1-5

MOS DEVICE MODELING AND CHARACTERIZATION
(Professional Elective – 4)

	L	T	P	C
I-M.Tech.-II-Sem.				
Course Code: 20VLPE205	**3**	**0**	**0**	**3**

Course Outcomes: Upon completion of the course, the students will be able to

1. discuss the threshold voltage modeling for 2-treminal MOS device.
2. analyze the C-V characteristics.
3. describe the threshold voltage modeling for 4-treminal MOS device.
4. illustrate the effect of sub-threshold modeling .
5. explain the SOI MOSFET structure

UNIT- I

2-terminal MOS device: threshold voltage modeling (ideal case as well as considering the effects of Q_f, Φ_{ms} and D_{it}.).

UNIT- II

C-V characteristics (ideal case as well as taking into account the effects of Qf, Qm and Dit); MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Qm and Dit)

UNIT- III

4-Terminal MOSFET: threshold voltage (considering the substrate bias); above threshold I-V modeling (SPICE level 1,2,3 and 4).

UNIT -IV

Sub threshold Modeling : current model; scaling; effect of threshold tailoring implant (analytical modeling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model)

UNIT- V

SOI MOSFET: basic structure; threshold voltage modeling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics

References:

1. D.G.Ong , "Modern MOS Technology: Processes, Devices and Design", McGraw Hill, 1984.
2. Y.Taur and T.H.Ning, "Fundamentals of modern VLSI Devices" Cambridge Univ. Press, 1998.
3. S.M.Sze, "Physics of Semiconductor Devices"Wiley,1981.

PHYSICAL DESIGN AUTOMATION
(Program Elective – 4)

	L	T	P	C
I-M.Tech.-II-Sem.				
Course Code: 20VLPE206	**3**	**0**	**0**	**3**

Course Outcomes: Upon completion of the course, the students will be able to

1. explain the concept of VLSI design automation tools
2. describe design rules and algorithms
3. discuss about floor planning and routing
4. outline the simulation and logic synthesis
5. analyze high-level synthesis

UNIT- I

VLSI Design Automation Tools: algorithms and system design. Structural and logic design.Transistor level design. Layout design. Verification methods. Design management tools.

UNIT- II

Design rules: Layout compaction, placement and routing. Design rules, symbolic layout.Applications of compaction.Formulation methods. Algorithms for constrained graph compaction. Circuit re-presentation. Wire length estimation. Placement algorithms. Partitioning algorithms.

UNIT- III

Floor Planning and Routing: floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.

UNIT- IV

Simulation and Logic Synthesis:gatelevel and switch level modeling and simulation.Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.

UNIT- V

High-Level Synthesis: Hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment and scheduling. Scheduling algorithms. Aspects of assignment. High level transformations.

Text Books:

1. S.H. Gerez, “Algorithms for VLSI Design Automation”, JohnWiley (India), 2006.
2. N.A.Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer, 2012.

References:

1. S.M. Sait, H. Youssef, “VLSI Physical Design Automation”, Cambridge India, 2010.
2. M.Sarrafzadeh, “Introduction to VLSI Physical Design”, McGraw Hill (IE), 1996.
3. Giovanni De Micheli, “Synthesis and Optimization of Digital Circuits”, McGraw Hill, 2017.
4. Andrew B. Kahng and Jens Lienig “VLSI Physical Design: From Graph Partitioning to Timing Closure”, Springer, 2011.
5. Recent literature in Physical Design Automation.

ANALOG AND DIGITAL CMOS VLSI DESIGN LAB

	L	T	P	C
I-M.Tech.-II-Sem.				
Course Code: 20VLPC203	**0**	**0**	**4**	**2**

Course Outcomes: Upon completion of the course, the students will be able to

1. design CMOS logic gates
2. design CMOS combinational circuits
3. develop CMOS sequential circuits
4. construct CMOS amplifiers
5. implement the CMOS SRAM cell

List of Experiments List of Experiments (Any **six** experiments from each part are to be conducted): **Transistor Level implementation of** CMOS **circuits using (180nm/90nm/45nm/Fin FET 18nm Technology)**

Part A : Digital CMOS VLSI Design

1. CMOS Buffer
2. CMOS NAND / NOR gates.
3. CMOS XOR
4. CMOS AND/OR gates
5. CMOS 28T Full Adder
6. CMOS 4:1 Multiplexer
7. CMOS Latch
8. CMOS Combinational circuits
9. CMOS Pass transistor
10. CMOS Complex circuits
11. CMOS 2:4 Decoder

Part B: Analog CMOS VLSI Design

1. CMOS Inverter
2. CMOS Common Source amplifier
3. CMOS Common Drain amplifier
4. CMOS Single stage Differential amplifier
5. CMOS Operational amplifier
6. CMOS SRAM CELL
7. CMOS D Flip-flop
8. CMOS SR Flip-flop
9. CMOS JK Flip-flop
10. CMOS T Flip-flop

References:

1. Analog and Digital CMOS VLSI Design Lab Manual, Department of ECE, CMRIT, Hyd.

VLSI DESIGN VERIFICATION AND TESTING LAB

	L	T	P	C
I-M.Tech.-II-Sem.				
Course Code: 20VLPC204	**0**	**0**	**4**	**2**

Course Outcomes: Upon completion of the course, the students will be able to

1. Simulate different classes and loops in System Verilog
2. Familiarity of Front end design and verification techniques and create reusable test environments
3. Verify increasingly complex designs more efficiently and effectively
4. Analyze, design and simulate digital circuits
5. Apply CAD tools for the design of digital circuits

List of Experiments ***(***Any **ten** experiments from each part are to be conducted):

1. Different classes in System Verilog
2. Different Loops in System Verilog
3. Random number functions
4. Pre-randomize and post -randomize functions
5. Single Port RAM Synchronous Read/Write
6. Synchronous/Asynchronous FIFO
7. Asynchronous/Synchronous reset D- FF
8. Semaphore
9. Mailbox
10. Parity
11. Device under Test
12. UART Scoreboard

References:

1.VLSI Design Verification And Testing Lab Manual, Department of ECE, CMRIT, Hyd,

MINI PROJECT WITH SEMINAR

	L	T	P	C
I-M.Tech.-II-Sem.				
Course Code: 20VLPR201	**0**	**0**	**4**	**2**

Mini Project will have mid semester presentation and end semester presentation. Mid semester presentation will include identification of the problem based on the literature review on the topic referring to latest literature available.

End semester presentation should be done along with the report on identification of topic for the work and the methodology adopted involving scientific research, collection and analysis of data, determining solutions highlighting individuals' contribution.

Continuous assessment of Mini Project at Mid Sem and End Sem will be monitored by the supervisor

PEDAGOGY STUDIES
(AUDIT COURSE - 2)

	L	T	P	C
I-M.Tech.-II-Sem.				
Course Code: 20AC201	**2**	**0**	**0**	**0**

OUTCOME: Students will be able to

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy

UNIT- I

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and Terminology, Theories of learning, Curriculum, Teacher education., Conceptual framework, Research questions**,** Overview of methodology and Searching.

UNIT- II

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries, Curriculum, Teacher education.

UNIT- III

Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies, How can teacher education (curriculum and practicum) and the school, curriculum and guidance materials best support effective pedagogy?, Theory of change., Strength and nature of the body of evidence for effective pedagogical practices., Pedagogic theory and pedagogical approaches., Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT-IV

Professional development: alignment with classroom practices and follow-up, support, Peer support, Support from the head teacher and the community., Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT- V.

Research gaps and future directions : Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

REFERENCE:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2):245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read'

STRESS MANGEMENT BY YOGA
(AUDIT COURSE - 2)

	L	T	P	C
I-M.Tech.-II-Sem.				
Course Code: 20AC202	**2**	**0**	**0**	**0**

UNIT-I:

Definitions of Eight parts of yoga. (Ashtanga)

UNIT-II:

Yam and Niyam.

UNIT-III:

Do`s and Don't's in life. i) Ahinsa, satya, astheya, bramhacharya and aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT-IV:

Asan and Pranayam

UNIT-V:

1. Various yoga poses and their benefits for mind & body
2. Regularization of breathing techniques and its effects-Types of pranayam

TEXT BOOKS/ REFERENCES:

1. "Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(AUDIT COURSE - 2)

I-M.Tech.-II-Sem. **L T P C**
Course Code: 20AC203 **2 0 0 0**

UNIT-I:

Neetisatakam-Holistic development of personality: Verses- 19,20,21,22 (wisdom), Verses- 29,31,32 (pride & heroism) Verses- 26,28,63,65 (virtue)

UNIT-II:

Neetisatakam-Holistic development of personality : Verses- 52,53,59 (dont's) Verses- 71,73,75,78 (do's)

UNIT-III:

Approach to day to day work and duties: Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48, Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35, Chapter 18-Verses 45, 46, 48.

UNIT-IV:

Statements of basic knowledge: Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 Chapter 12 - Verses 13, 14, 15, 16,17, 18 Personality of Role model.

UNIT-V:

Shrimad Bhagwad Geeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42, Chapter 4-Verses 18, 38,39 Chapter18 – Verses 37,38,63

TEXT BOOKS/ REFERENCES:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

II-M.TECH.-I-SEMESTER SYLLABUS

MICROCHIP FABRICATION TECHNIQUES
(Professional Elective – 5)

	L	T	P	C
II-M.Tech.-I-Sem.				
Course Code: 20VLPE301	**3**	**0**	**0**	**3**

Course Outcomes: On completion of this course, students are able to

1. Discuss basic wafer fabrication operations
2. Illustrate different techniques of Cleanroom Technology.
3. Examine the different types of CVD process.
4. Design rules and Scaling of BICMOS ICs
5. Describe about Packaging.

UNIT-I
O**verview of Semiconductor Industry:** Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources

UNIT-II
Cleanroom Technology: Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization. Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping, Doping and depositions: Diffusion process steps, deposition

UNIT-III
Doping and Depositions: Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems
Plasma enhanced CVD systems, Vapour phase epitoxy, molecular beamepitaxy.

UNIT-IV
Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors

UNIT-V
Packaging: Chip characteristics, package functions, package operations

Text Books:
1. Peter Van Zant, Microchip fabrication, McGraw Hill,1997.
2. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY,1988
3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press,2000
4. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill,2000

DESIGN FOR TESTABILITY
(Professional Elective – 5)

	L	T	P	C
II-M.Tech.-I-Sem.				
Course Code: 20VLPE302	**3**	**0**	**0**	**3**

Course Outcomes: On completion of this course, students are able to

1. Discuss the Scope of testing and verification in VLSI design process
2. Explain Fundamentals of VLSI testing and scan based design.
3. Analyze BIST for testing of logic and memories.
4. Design test automation for functional verification
5. Describe about Testing Models.

UNIT- I

Basics of Testing: Scope of testing and verification in VLSI design process. Issues in test and verification of complex chips, embedded cores and SOCs.

UNIT- II

Fundamentals of VLSI Testing.: Fault models. Automatic test pattern generation. Design for testability. Scan design. Test interface and boundary scan.

UNIT- III

Built-in Self-Test: System testing and test for SOCs. Iddq testing. Delay fault testing, BIST for Testing of logic and memories.

UNIT- IV

Test Automation: Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification.

UNIT- V

Testing Models : Basics of equivalence checking and model checking. Hardware emulation. Parametric testing, Reliability modeling, Yield models.

Text Books:

1. M. Bushnell and V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer AcademicPublishers,2000
2. M. Abramovici, M. A. Breuer and A. D. Friedman, “Digital Systems Testing and Testable Design, IEEE”, IEEE Press,1990
3. T. Krop, “Introduction to Formal Hardware Verification”, SpringerVerlag,,2000
4. P. Rashinkar, Paterson and L. Singh, “System-on-a-Chip Verification-Methodology and Techniques”, Kluwer Academic Publishers,2001.
5. Jan M. Rabaey, “Digital Integrated Circuits”, Prentice Hall,2003.
6. M.J.S. Smith, “Application Specific Integrated Circuits”, Pearson Education India,1997
7. Alfred L. Crouch “Design for test for digital ICs and embedded core systems” , PHI1999

NANOMATERIALS AND NANOTECHNOLOGY
(Professional Elective – 5)

	L	T	P	C
II-M.Tech.-I-Sem.				
Course Code: 20VLPE303	**3**	**0**	**0**	**3**

Course Outcomes: On completion of this course, students are able to

1. Discuss the types of Nanomaterials.
2. Relate nano-materials for different applications.
3. Examine MEMS and quantum dots .
4. Propose Carbon nanotubes for memories.
5. Organize Nano Electronics for Quantum computers

UNIT-I:

Introduction to Nanomaterials: nanomaterials in one and higher dimensions: Types of Nano-Materials, Special Magnetic Nanomaterials, Quantum mechanical Properties, Nanomaterials in dimensions

UNIT-II

Applications of Nanomaterials: Applications of one and higher dimension nanomaterials, Magneto Resistance effects in magnetic materials, Spin Valve Effect, Medical Nanomaterials

UNIT-III

Fabrication of MEMS: Lithography,Some Tools of Micro Nano Fabrication micro electro-mechanical system (MEMS) ,nano-phonics: Optical Nano materials Excitons, band-gap variations-quantum confinement (quantum dots)

UNIT-IV

Carbon Nanotubes : synthesis, Fictionalization and applications: CNT-FET, Memories.

UNIT-V

NANO Physics and NANO Electronics: SET, FinFET, Quantum computers,Optical Nanomaterials.

Text Books:

1. Nanoscale Materials in Chemistry edited by Kenneth J. Klabunde and Ryan M. Richards, 2nd edn, John Wiley and Sons, 2009.
2. Nan crystalline Materials by A I Gusev and A ARempel, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
3. Springer Handbook of Nanotechnology by Bharat Bhushan, Springer, 3rdedn, 2010.
4. Carbon Nanotubes: Synthesis, Characterization and Applications by Kamal K. Kar, Research Publishing Services; 1stedn, 2011, ISBN-13: 978-9810863975.

COMPOSITE MATERIALS
(Open Elective)

II-M.Tech.-I-Sem. **L T P C**
Course Code: 20MEOE301 **3 0 0 3**

Course outcomes: At the end of the course, students will be able to

1. outline the characteristics and effect of reinforcement in composite materials.
2. illustrate the various fiber reinforcement properties and its application.
3. discuss the manufacturing process of metal matrix composites.
4. analyze the various methods for polymer matrix composites.
5. determine the various failure of composite materials.

UNIT–I

Introduction: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT – II

Reinforcements: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT – III

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT–IV

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

UNIT – V

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

Text Books:

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R.Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.

CONSTRUCTION MANAGEMENT
(Open Elective)

	L	T	P	C
II-M.Tech.-I-Sem.				
Course Code: 20CEOE302	**3**	**0**	**0**	**3**

Course outcomes: At the end of the course, students will be able to

1. outline basic concepts of planning, strategy implementation and human resource management
2. adopt the scientific method of management for various construction projects
3. identify the different resources such as manpower, materials, cost and equipment
4. elaborate the contract document , specification and billing system
5. discuss the labour regulation, administration, accident, safety and legal issues

UNIT -I

Management process- Roles. Management theories. Social responsibilities. Planning and strategic management. Strategy implementation. Decision making: tools and techniques – Organizational structure. Human resource management- motivation performance- leadership.

UNIT-II

Classification of Construction projects, Construction stages, Resources- Functions of Construction Management and its Applications .Preliminary Planning- Collection of Data-Contract Planning – Scientific Methods of Management: Network Techniques in construction management - Bar chart, Gant chart, CPM, PERT- Cost & Time optimization.

UNIT-III

Resource planning - planning for manpower, materials, costs, equipment. Labour, -Scheduling .Forms of scheduling - Resource allocation. budget and budgetary control methods

UNIT-IV

Contract - types of contract, contract document, and specification, important conditions of contract – tender and tender document - Deposits by the contractor - Arbitration . negotiation - M.Book - Muster roll -stores.

UNIT-V

Management Information System - Labour Regulations: Social Security - welfare Legislation - Laws relating to Wages, Bonus and Industrial disputes, Labour Administration - Insurance and Safety Regulations - Workmen's Compensation Act -other labour Laws - Safety in construction: legal and financial aspects of accidents in construction. occupational and s`afety hazard assessment. Human factors in safety. Legal and financial aspects of accidents in construction. Occupational and safety hazard assessment

Reference:

1. Ghalot, P.S., Dhir, D.M., Construction Planning and Management, Wiley Eastern Limited,1992.
2. Chitkara,K.K.,Construction Project Management¸Tata McGraw Hill Publishing Co,Ltd.,New Delhi.
3. Punmia,B,C., Project Planning and Control with PERT and CPM, Laxmi Publications, New Delhi.
4. Sengupta, B. & Guha, H, Construction Management And Planning by: Tata McGraw-hill publications.

VLSI DESIGN
(Open Elective)

II-M.Tech.-I-Sem. **L T P C**
Course Code: 20ECOE303 **3 0 0 3**

Course Outcomes: Upon completion of the course, the students will be able to

1. interpret various MOS transistor fabrication techniques
2. illustrate the operation and electrical characteristics of MOS transistor
3. discuss VLSI Design flow, Stick diagrams, layout, design rules of MOS transistor
4. outline the basic concepts of MOS circuits
5. interpret scaling of MOS transistor and various levels of CMOS testing

UNIT -I
Introduction: Introduction to IC technology, Basic MOS transistors, Enhancement and depletion modes of transistor action. Fabrication process of NMOS, PMOS,CMOS and Bi-CMOS technology and comparison between CMOS and bipolar technologies.

UNIT -II
Basic Electrical properties of MOS circuits: Basic Electrical Properties of MOS and BiCMOS Circuits: Ids-Vds relationships, MOS transistor threshold Voltage, gm, gds. CMOS Inverter analysis and design, Bi-CMOSInverters.MOS Transistor conductance and output conductance, MOS transistor figure of merit, Pass transistors, nMOS inverter , Determination of pull up to pull down ratio for an nMOS inverter driven by another nMOS inverter and for an nMOS inverter driven through one or more pass transistors, Alternate forms of pull up, CMOS inverter, BiCMOS Inverters.

UNIT-III
VLSI Circuit Design Processes: VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules and Layout, 2μm CMOS Design rules for wires, Contacts and Transistors.Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits.

UNIT-IV
Basic concepts of MOS Circuits: Sheet resistance, Sheet resistance concept applied to MOS transistors and inverters, Area capacitance of layers , standard unit of capacitance, some area capacitance calculations, The delay unit, inverter delays, Driving large capacitance loads, Propagation delays, wiring capacitances, Fan-in and Fan-out characteristics, Choice of layers, CMOS steady state electrical behavior, CMOS dynamic electrical behavior.
UNIT-V
Scaling of MOS Circuits: Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling.
CMOS Testing: Need for CMOS testing, design strategies for test Manufacturing test principles, Design for testability (DFT) - Adhoc testing, Scan design, Built in self-test (BIST).

Textbooks:

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Dougles A. Pucknell, PHI, 2005.
2. CMOS VLSI Design – A Circuits and Systems Perspective, Neil H. E Weste, David Harris, Ayan Banerjee, 3rd Ed, Pearson, 2009.

References:

1. CMOS logic circuit Design - John. P. Uyemura, Springer.
2. Modern VLSI Design - Wayne Wolf, Pearson Education.

DATA MINING AND ANALYTICS
(Open Elective - I)

M.Tech. II Year-I Sem **L T P C**
Course Code: 20CSOE304 **3 0 0 3**

Course Outcomes: Upon completion of the course, the student will be able to

1. summarize fundamentals of data mining
2. illustrate various mining association rules
3. make use of classification and clustering techniques
4. outline various data analytics techniques
5. solve statistical problems using R programming

Unit-I

Introduction to Data Mining: Kinds of Data, Data mining Functionalities – Interesting Patterns Task Primitives, Issues in Data Mining, Data Preprocessing.

Unit-II

Mining Frequent, Associations and Correlations: Basic Concepts, Frequent Itemset Mining Methods:, Apriori Algorithm: Finding Frequent Itemsets by Confined Candidate Generation, Generating Association Rules from Frequent Itemsets, Improving the Efficiency of Apriori, From Association Analysis to Correlation Analysis.

Unit-III

Classification: Basic Concepts, Algorithm for Decision Tree Induction, Attribute Selection Measures. Bayes Classification Methods, Bayesian Belief Networks, a Multilayer Feed-Forward Neural Network, k-Nearest-Neighbor Classifiers.
Clustering: Cluster Analysis, Partitioning Methods: k-Means and k-Medoids, Hierarchical Methods: Agglomerative versus Divisive Hierarchical Clustering.

Unit-IV

Data Definitions and Analysis Techniques: Introduction to statistical learning and R-Programming, Elements, Variables, and Data categorization, Levels of Measurement, Data management and indexing.

Unit-V

Basic Analysis Techniques: Statistical hypothesis generation and testing, Chi-Square test, t-Test, Analysis of variance, Maximum likelihood test, regression, Practice and analysis with R.

Textbooks:

1. Data Mining- Concepts and Techniques- Jiawei Han, Micheline Kamber, Morgan Kaufmann Publishers, Elsevier, 2 Edition, 2006.
2. Introduction to Data Mining, Pang-Ning Tan, Vipin Kumar, Michael Steinbanch, Pearson Education.
3. An Introduction to Statistical Learning: with Applications in R, G James, D. Witten, T Hastie, and R. Tibshirani, Springer, 2013

References:

1. Data mining Techniques and Applications, Hongbo Du Cengage India Publishing
2. Data Mining Techniques, Arun K Pujari, 3rd Edition, Universities Press.
3. Software for Data Analysis: Programming with R (Statistics and Computing), John M. Chambers, Springer.

PROJECT – I / DISSERTATION PHASE – I

	L	T	P	C
II-M.Tech.-I-Sem.				
Course Code: 20VLPR301	**0**	**0**	**20**	**10**

Dissertation-I will have mid semester presentation and end semester presentation. Mid semester presentation will include identification of the problem based on the literature review on the topic referring to latest literature available.

End semester presentation should be done along with the report on identification of topic for the work and the methodology adopted involving scientific research, collection and analysis of data, determining solutions and must bring out individuals contribution.

Continuous assessment of Dissertation – I and Dissertation – II at Mid Sem and End Sem will be monitored by the departmental committee.

II-M.TECH.-II-SEMESTER SYLLABUS

PROJECT – II / DISSERTATION PHASE – II

	L	T	P	C
II-M.Tech.-II-Sem.				
Course Code: 20VLPR401	**0**	**0**	**32**	**16**

Dissertation – II will be an extension of the topic identified in Dissertation – I.
Continuous assessment should be done of the work done by adopting the methodology decided involving numerical analysis/ conduct experiments, collection and analysis of data, etc. There will be pre submission seminar at the end of academic term. After the approval the student has to submit the detail report and external examiner is called for the viva-voce to assess along with guide.