ACADEMIC REGULATIONS (R22)

COURSE STRUCTURE AND DETAILED SYLLABUS

(CHOICE BASED CREDIT SYSTEM (CBCS))

M.Tech. - VLSI

(Applicable for the batches admitted from 2022 - 2023)

Department of Electronics and Communication Engineering

CMR INSTITUTE OF TECHNOLOGY

(UGC - Autonomous)

Approved by AICTE, Permanently Affiliated to JNTUH, Accredited by NBA and NAAC with A Grade

Kandlakoya(V), Medchal District, Hyderabad-501 401, Telangana State

Mobile No.: 8008557612 **E-mail:** principal@cmritonline.ac.in **Web:** www.cmritonline.ac.in

FOREWORD

CMR Institute of Technology, established in the year 2005, Approved by AICTE, New Delhi, Permanently Affiliated to JNTUH, Accredited by NBA under Tier-I, Achieved UGC Autonomous Status and has been bestowed with NAAC 'A' Grade for its remarkable academic accomplishments accompanied by its unflinching spirit and dedication to impart quality technical education to the deserving aspirants. The institution has commenced functioning independently within the set norms prescribed by UGC and AICTE. The performance of the institution manifests the confidence that the prestigious monitoring body, the UGC has on it, in terms of upholding its spirit and sustenance of the expected standards of functioning on its own consequently facilitating the award of degrees for its students. Thus, an autonomous institution is provided with the necessary freedom to have its own **curriculum, examination system and monitoring mechanism**, independent of the affiliating University but under its observance.

CMR Institute of Technology takes pride for having won the confidence of such distinguished academic bodies meant for monitoring the quality in technology education. Besides, the institution is delighted to sustain the same spirit of discharging the responsibilities that it has been conveying since 2005 to attain the current academic excellence in improvement of the standards and ethics. Institutional Governance enriched by eminent personalities on many of its boards/councils such as the Governing Body, Academic Council, Boards of Studies, IQAC to frame the guidelines for curriculum design and development in the interest of the key-stakeholders.

The autonomous academic regulations, course structure and syllabi have been framed in accordance with the vision and mission of the institution on the valuable suggestions from various stakeholders from the diverse fields of academics, industry, R&D and society with a bird-eye-view to impart quality professional technical education to contribute the society with innovation and creativity.

All the staff members, parents and students are requested to study all the rules and regulations carefully and approach the Principal to seek any clarifications, if needed, without presumptions, to avoid unwanted subsequent embarrassments. The cooperation of all the stakeholders is sought for the successful implementation of the autonomous system in the larger interests of the institution and for brightening the career prospects of engineering and management graduates.

———

INDEX

CMR INSTITUTE OF TECHNOLOGY

Vision: To create world class technocrats for societal needs.

Mission: Achieve global quality technical education by assessing learning environment through

- Innovative Research & Development
- Eco-system for better Industry institute interaction
- Capacity building among stakeholders

Quality Policy: Strive for global professional excellence in pursuit of key-stakeholders.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING (ECE)

Vision: To become pioneer in the field of electronics & communication engineering by providing creative and innovative solutions for societal needs.

Mission: The department of **Electronics and Communication Engineering** is committed to

- Provide excellence in education, research and extension services.
- Provide quality education and to make the students entrepreneurs and employable.
- Learn continuously the state-of-art technologies for global excellence.

M.Tech. - VLSI

I. Programme Educational Objectives (PEOs): Engineering Graduates will

1. Pursue successful career in the field of VLSI design.
2. Pursue lifelong learning for research and innovative skills to solve problems in VLSI domain.
3. Exhibit professionalism, ethics, inter-personal skills and leadership.

II. Programme Outcomes (POs): Engineering Graduates will have ability to

1. Carry out investigation, research, development and solve complex problems independently.
2. Write, present and substantiate a technical report/document.
3. Demonstrate mastery in the field of VLSI.

III. Programme Specific Outcomes (PSOs): Engineering Graduates will be able to

1. Design fault tolerant VLSI circuits to optimize power and area requirements.
2. Develop technically-feasible and environmentally-sustainable VLSI systems.

_____

M.Tech. - Academic Regulations - R22
(For batches admitted from the Academic Year 2022 - 23)

PREAMBLE

For pursuing M.Tech. - Regular Two Year Post Graduate Degree Programme offered by **CMR Institute of Technology (CMRIT)** under Autonomous status will herein be referred to as CMRIT (Autonomous).

All the specified rules are herein approved by the Academic Council. These rules will be in force and are applicable to students admitted from the academic year 2022-23 onwards. Any reference to "**Institute**" or "**College**" in these rules and regulations stand for CMRIT (Autonomous).

All the rules and regulations specified shall hereafter be read as a whole for the purpose of interpretation, as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, CMRIT (Autonomous) shall be The Chairman, Academic Council.

1. POST-GRADUATE DEGREE PROGRAMMES IN ENGINEERING & TECHNOLOGY (PGP IN E&T)

CMR Institute of Technology offers **Two** Years (**Four** Semesters) full-time Master of Technology (M.Tech.) Degree Programmes, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.

2. ELIGIBILITY FOR ADMISSIONS

2.1 Admission to the PGPs shall be made subject to eligibility, qualification and specializations prescribed by the JNTUH from time to time, for each specialization under each M.Tech. Programme.

2.2 Admission to the post graduate programme shall be made on the basis of either the merit rank or Percentile obtained by the qualified student in there relevant qualifying GATE Examination/the merit rank obtained by the qualified student in an entrance test conducted by Telangana State Government(PGECET) for M.Tech. Programmes /an entrance test conducted by JNTUH/on the basis of any other exams approved by the JNTUH, subject to reservations as laid down by the Govt. from time to time.

2.3 The medium of instructions for all PG Programmes will be **English** only.

3. M.Tech. PROGRAMME (PGP in E&T) STRUCTURE

3.1 The M.Tech. Programs in E & T of JNTUH are of Semester pattern, with **Four** Semesters consisting of **Two** academic years, each academic year having **Two** Semesters (First/Odd and Second/Even Semesters). Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per Semester.

3.2 The two-year M.Tech. Program consists of **68** credits and the student has to register for all **68** credits and earn all **68** credits for the award of M.Tech. degree. There is **NO** exemption of credits in any case.

3.3 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M.Tech. degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M.Tech. Programme.

3.4 **UGC/AICTE** specified definitions/descriptions are adopted appropriately for various terms and abbreviations used in these PG academic regulations, as listed below:

3.4.1 Semester Scheme:

Each Semester shall have 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) are taken as 'references' for the present set of Regulations. The terms 'SUBJECT'/'COURSE' imply the same meaning here and refer to 'Theory/Lab Course'/ 'Design/Drawing Subject'/'Mini Project with Seminar'/'Dissertation', as the case may be.

3.4.2 Credit Courses:

All Subjects/Courses are to be registered by a student in a Semester to earn Credits. Credits shall be assigned to each Subject/Course in a L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods: Credits) Structure based on the following pattern:

Theory		Practical	
1 Hr. Lecture (L) per week	1 credit	1 Hr. Practical (P) per week	0.5 credit
1 Hr. Tutorial (T) per week	1 credit	2 Hrs Practical (Lab) per week	1.0 credit

All Mandatory Courses, Study Tour, Guest Lecture, etc., will not carry any Credits.

Contact Hours: Weekly contact hours – maximum of 30 hours per week (i.e. 1 hour = 60 Minutes) including credit and non-credit courses.

3.4.3 Subject/ Course Classification:

All subjects/courses offered for the Post-Graduate Programme in E & T (M.Tech. Degree Programme) are broadly classified as follows. The JNTUH has followed in general the guidelines issued by AICTE/UGC.

S. No.	Broad Course Classification	Course Group/Category	Course Description
1	Core Courses (CoC)	PC- Professional Core	Includes subjects related to the parent discipline/department/branch of Engineering.
		Dissertation	M.Tech. Project or PG Project or Major Project.
		Mini Project with Seminar	Seminar based on core contents related to Parent Discipline/Department/Branch of Engineering.
2	Elective Courses(EℓC)	PE- Professional Electives	Includes elective subjects related to the parent discipline/department/branch of Engineering.
		OE- Open Electives	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline/department/ branch of Engineering.
3	***MC - Mandatory Courses***		***Non-Credit Audit Courses***

4. COURSE REGISTRATION

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each specialization, who will advise on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice/Option for Subjects/Courses, based on his competence, progress, pre-requisites and interest.

4.2 The Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work through 'ON-LINESUBMISSIONS', ensuring 'DATE and TIME Stamping'. The ON-LINE Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply for ON-LINE Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it be in retained with Head of Department, Faculty Advisor and the Student).

4.4 If the student submits ambiguous choices or multiple options or erroneous entries during ON-LINE Registration for the Subject(s)/Course(s) under a given/specified Course Group/Category as listed in the Course Structure, only the first mentioned Subject/Course in that Category will be taken into consideration.

4.5 Subject/Course Options exercised through ON-LINE Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices also will not be considered. However, if the Subject/Course that has already been listed by the CMRIT in a semester could not be offered due to unforeseen or unexpected reasons, then the student will be allowed to have alternate choice either for a new subject, if it is offered, or for another existing subject. Such alternate arrangements will be made by the Head of Dept., with due notification and time-framed schedule, with in the FIRST WEEK from the commencement of class-work for that Semester.

5. ATTENDANCE REQUIREMENTS

The programmes are offered based on a unit system with each subject being considered a unit. Attendance is calculated separately for each subject.

5.1 Attendance in all courses is compulsory. The minimum required attendance in each theory/lab subject (***also mandatory Audit Courses***) including the attendance of mid-term examination/ Laboratory etc. is 75%. Two periods of attendance for each theory subject shall be considered, if the student appears for the mid-term examination of that subject. A student shall not be permitted to appear for the SEE, if his attendance is less than 75%.

5.2 A student's Seminar report and presentation on Mini Project shall be eligible for evaluation, only if he ensures a minimum of 75% of his attendance in Seminar presentation classes on Mini Project during that Semester.

5.3 **Condoning of shortage of attendance** (between 65% and 75%) up to a maximum of 10% (considering the days of attendance in sports, games, NCC, NSS activities and Medical grounds) in each subject (Theory/Lab/Mini Project with Seminar) of a semester shall be granted by the College Academic Committee on genuine reasons.

5.4 A prescribed fee per subject shall be payable for condoning shortage of attendance after getting the approval of College Academic Committee for the same. The College Academic Committee shall maintain relevant documents along with the request from the student.

5.5 Shortage of Attendance below 65% in any subject shall in **no case be condoned.**

5.6 A Student, whose shortage of attendance is not condoned in any Subject(s) (Theory/Lab/Mini Project with Seminar) in any Semester, is considered as 'Detained in that Subject(s), and is not eligible to write SEE of such Subject(s); in case of 'Mini Project with Seminar, without a Report or Presentation are not eligible for evaluation in that semester; and the student have to seek re-registration for those subject(s) in subsequent semesters and attend the same as and when offered.

5.7 A student fulfills the attendance requirement in the present semester, shall not be eligible for readmission into the same class.

5.8 **a)** A student shall put in a minimum required attendance in at least **three theory subjects (excluding *mandatory (non-credit audit)* course)** in I semester for promotion to II Semester.

b) A student shall put in a minimum required attendance in at least **three theory subjects (excluding *mandatory (non-credit audit)* course)** in II semester for promotion to III Semester.

6. ACADEMIC REQUIREMENTS

The following academic requirements must be satisfied, in addition to the attendance requirements mentioned in itemno.5. The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks per subject/course (theory/practical), based on Continuous Internal Evaluation (CIE) and Semester End Examination (SEE).

6.1 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course, if he secures not less than (i) 40% of Marks (24 out of 60 marks) in the Semester End Examination (ii) 40% of Marks in the internal examinations (16out of 40 marks allotted for CIE); and (iii) A minimum of 50% of marks in the sum total of CIE and SEE taken together; in terms of Letter Grades this implies securing **'B'** Grade or above in a subject.

6.2 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to Mini Project with seminar, if student secures not less than 50% marks (i.e. 50 out of 100 allotted marks). The student would be treated as failed, if student (i) does not submit a seminar report on Mini Project or does not make a presentation of the same before the evaluation committee as per schedule or (ii) secures less than 50% marks in Mini Project with seminar evaluation. The failed student shall reappear for the above evaluation when the notification for supplementary examination is issued.

6.3 A student shall register for all subjects for total of **68** credits as specified and listed in the course structure for the chosen specialization, put in the required attendance and fulfill the academic requirements for securing **68** credits obtaining a minimum of 'B' Grade or above in each subject, and all **68** credits securing Semester Grade Point Average **(SGPA)** $\geq$ **6.0** (in each semester) and final Cumulative Grade Point Average **(CGPA)** (i.e., CGPA at the end of PGP**)** $\geq$ **6.0**, and shall ***pass all the mandatory Audit Courses*** to complete the PGP successfully.

Note:(1) The SGPA will be computed and printed on the marks memo only if the candidate passes in all the subjects offered and gets minimum B grade in all the subjects.

(2) CGPA is calculated only when the candidate passes in all subjects in all semesters.

6.4 Marks and Letter Grades obtained in all those subjects covering the above specified **68** credits alone shall be considered for the calculation of final CGPA, which will be indicated in the Grade Card/Marks Memo of second year second semester.

6.5 If a student registers for extra subject(s) (in the parent department or other departments/ branches of Engineering) other than those listed subjects totaling to **68** credits as specified in the course structure, the performance in extra subject(s) (although evaluated and graded using the same procedure as that of the required **68** credits) will not be considered while calculating the SGPA and CGPA. For such extra subject(s) registered, percentage of marks and Letter Grade alone will be indicated in the Grade Card/Marks Memo, as a performance measure, subject to completion of the attendance and academic requirements as stated in items 5 and 6.1-6.3.

6.6 When a student is detained due to shortage of attendance in any subject(s) in any semester, no Grade allotment will be made for such subject(s). However, he is eligible for re-registration of such subject(s) in the subsequent semester(s), as and when next offered, with the academic regulations of the batch into which he is re-registered, by paying the prescribed fees per subject. In all these re-registration cases, the student shall have to secure a fresh set of internal marks and SEE marks for performance evaluation in such subject(s), and SGPA/CGPA calculations.

6.7 A student eligible to appear for the Semester End Examination in any subject, but absent from it or failed (failing to secure 'B' Grade or above), may reappear for that subject at the supplementary examination as and when conducted. In such cases, his Internal Marks assessed earlier for that subject will be carried over, and added to the marks secured in the supplementary examination, for the purpose of evaluating his performance in that subject.

6.8 A student who fails to earn **68** credits as per the specified course structure, and as indicated above, within **four** academic years from the date of commencement of his first year first semester, shall forfeit his seat in M.Tech. Programme and his admission **shall stand cancelled.**

7. EVALUATION - DISTRIBUTION AND WEIGHTAGE OF MARKS

The performance of a student in each semester shall be evaluated subject-wise (irrespective of credits assigned) for a maximum of 100 marks.

7.1 The performance of a student in every subject/course (including practical's and Project) will be evaluated for 100 marks each, with 40 marks allotted for CIE and 60 marks for SEE. The CIE shall be made based on the average of the marks secured in the two Mid-Term Examinations conducted, first Mid-Term examinations in the middle of the Semester and second Mid-Term examinations during the last week of instruction.

7.2 **Evaluation of Theory Subjects/Courses**

A) Continuous Internal Evaluation (CIE): In CIE, for theory subjects, during a semester, there shall be **Two** Mid-Term Examinations. The first Mid-Term Examination shall be conducted for the first 50% of the syllabus, and the Second Mid-Term for the remaining 50% of the syllabus. Each Mid-Term examination consists of two parts (i) **Part - A** for 5 marks, (ii) **Part - B** for 25 marks with a total duration of 2 hours as follows:

- Part-A consists of one compulsory question with five sub questions carrying one mark each and Part-B consists of 5 essay questions with internal choice carrying five marks each; the student has to answer all 5 questions. The First and Second Mid-Term question papers comprise of 2,2,1 questions from I, II, III(A) Units and 1,2,2 questions from III(B), IV, V Units respectively. The **average of two Mid Term Examinations** shall be taken as final marks for Mid-Term Examination (for 30 marks).
- The remaining 10 marks of CIE are distributed as follows:
  - (i) Assignment for 5 marks. First assignment should be submitted before the commencement of the first mid-term examinations and the second assignment before the commencement of second mid-term examinations. The assignments shall be specified/given by the concerned subject teacher. The average of two assignments shall be taken as final marks for assignment (for 5 marks).
  - (ii) Subject Viva-Voce/PPT/Poster Presentation/Case Study on a topic in the subject concerned for 5 marks before commencement of II Mid-Term Examination.
- The Student, in each subject, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

B) Semester End Examinations (SEE): The duration of SEE is 3 hours. The details of the question paper pattern are as follows:

- The end semester examinations will be conducted for 60 marks consisting of two parts viz. i) **Part- A** for 10 marks, ii) **Part - B** for 50 marks.
- Part-A is compulsory, which consists of ten questions (two from each unit) carrying 1 mark each.
- Part-B consists of five questions (numbered from 11 to 15) carrying 10 marks each. One question from each unit (may contain sub-questions) with internal choice.

7.3 **Evaluation of Practical Subjects/Courses:** For practical subjects there shall be a CIE during the semester for 40 marks and 60 marks for SEE. Out of the 40 marks for CIE:

A) Continuous Internal Evaluation (CIE): The distribution of CIE 40 marks for practical subjects is as follows:

1. A write-up on day-to-day experiment(s) in the laboratory shall be evaluated for 15 marks. The breakup of marks would be (i) 3 marks for observation and record (ii) 4 marks for performance of experiment (iii) 3 marks for expected outcome and (iv) 5 marks for Viva-Voce. The average marks of day-to-day experiments shall be the final marks (for 15 marks).

2. Internal practical examination conducted by the laboratory teacher concerned shall be evaluated for 15 marks. The breakup of marks are (i) 3 marks for write-up (ii) 4 marks for experiment/program (iii) 3 for evaluation of results and (iv) 5 marks for viva-voce on concerned laboratory course.
3. The remaining 10 marks are for Laboratory Project, which consists of the Design (or) Software/Hardware Model Presentation (or) App Development (or) Prototype Presentation submission which shall be evaluated after completion of laboratory course and before Semester End Practical Examination.

B) Semester End Examination (SEE): The Semester End Examination (SEE) for practical subject/course shall be conducted at the end of the semester with duration of 3 hours by one internal and one external examiner appointed by the Head of the Institution as per the recommendation of the concerned Head of the Department for 60 marks. The allocation of marks is as given below:

- (i) 10 marks for write-up (ii) 15 marks for experiment/program (iii) 15 marks for evaluation of results (iv) 10 marks for presentation on another experiment/program in the same lab course and (v) 10 marks for viva-voce on concerned laboratory course.

7.4 **Condition for Passing CIE and SEE in Theory and Practical Subject(s)/Course(s):** The Student, in each subject, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks put together.

- The student is eligible to write Semester End Examination of the concerned subject, if the student scores ≥ 40% (16 marks) of 40 Continuous Internal Examination (CIE) marks.
- In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

7.5 For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Principal within two weeks, before commencement of the lab SEE. The external examiner should be selected from outside the college concerned but within the cluster. No external examiner should be appointed from any other college in the same cluster/any other cluster which is run by the same Management.

7.6 There shall be Mini Project with Seminar during II semester for internal evaluation of 100 marks. The Departmental Academic Committee (DAC) will review the progress of the mini project during the seminar presentations and evaluate the same for 50 marks. Mini Project Viva Voce will be evaluated by the DAC for another 50 marks before the SEE. Student shall carryout the mini project in consultation with the mini project supervisor which may include critically reviewing the literature, project implementation and submit it to the department in the form of a report and shall make an oral presentation before the DAC consisting of Head of the Department, Mini Project supervisor and two other senior faculty members of the department. The student has to secure a minimum of 50% of marks in i) seminar presentation and ii) mini project viva voce, to be declared successful. If he fails to obtain the minimum marks, he has to reappear for the same as and when scheduled.

7.7 Every candidate shall be required to submit a dissertation on a topic approved by the Dissertation Review Committee.

7.8 A DRC shall be constituted with the Head of the Department as Chairperson, Dissertation Supervisor and one senior faculty member of the Department offering the M.Tech. Programme.

7.9 Registration of Dissertation Work: A candidate is permitted to register for the Dissertation Work after satisfying the attendance requirement in all the subjects, both theory and laboratory.

7.10 After satisfying 7.9, a candidate must present in **Dissertation Work Review-I**, in consultation with his Dissertation Supervisor, the title, objective and plan of action of his Dissertation work to the DRC for approval **within four weeks** from the commencement of **III Semester**. Only after obtaining the approval of the DRC can the student initiate the Dissertation work.

7.11 If any candidate wishes to change their supervisor or topic of the dissertation, they can do so with the approval of the DRC. However, the DRC shall examine whether or not the change of topic/supervisor leads to a major change in initial plans of dissertation proposal and the date of registration for the project work starts from the date of change of supervisor or topic.

7.12 A candidate shall submit his Dissertation progress report in two stages at least with a gap of **three** Months between them.

7.13 The work on the dissertation shall be initiated at the beginning of the III semester and the duration of the Dissertation is two semesters. A candidate is permitted to submit Dissertation Thesis only after successful completion of all theory and practical courses with the approval of DRC **not earlier than 40 weeks** from the date of approval of the Dissertation work. For the approval of DRC, the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the DRC.

7.14 **The Dissertation Work Review-II** in III Semester carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and DRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Dissertation Work. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - II. If he fails to obtain the minimum required marks, he has to reappear for Dissertation Work Review-II as and when conducted.

7.15 **The Dissertation Work Review-III** in IV Sem. Carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The DRC will examine the overall progress of the Dissertation Work and decide whether or not the Dissertation is eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Dissertation Work Review - III as and when conducted. For Dissertation Evaluation (Viva Voce) in IV Semester there are external marks of 100 and it is evaluated by the external examiner. The candidate has to secure a minimum of 50% marks in Dissertation Evaluation (Viva-Voce) examination.

7.16 Dissertation Work Reviews-II and III shall be conducted in phase I (Regular) and Phase II (Supplementary). Phase II will be conducted only for unsuccessful students in Phase I. The unsuccessful students in Dissertation Work Review - II (Phase II) shall reappear for it at the time of Dissertation Work Review-III (Phase I). These students shall reappear for Dissertation Work Review - III in the next academic year at the time of Dissertation Work Review - II only after completion of Dissertation Work Review - II, and then Dissertation Work Review - III follows. The unsuccessful students in Dissertation Work Review - III (Phase II) shall reappear for Dissertation Work Review – III in the next academic year only at the time of Dissertation Work Review –II (Phase I).

7.17 After approval from the DRC, a soft copy of the thesis should be submitted for ANTI-PLAGIARISM check and the plagiarism report should be submitted to the HOD and be included in the final thesis.

The Thesis will be accepted for submission, if the similarity index is less than **30%**.If the similarity index has more than the required percentage, the student is advised to modify accordingly and re-submit the soft copy of the thesis after one month. The maximum number of re-submissions of thesis after plagiarism check is limited to **TWO**. The candidate has to register for the Dissertation work and work for two semesters. After three attempts, the admission is liable to be cancelled. The college authorities are advised to make plagiarism check of every soft copy of theses before submissions.

7.18 Three copies of the Dissertation Thesis certified by the supervisor shall be submitted to the College/School/Institute, after submission of a research paper related to the Dissertation work in a UGC approved journal. A copy of the submitted research paper shall be attached to thesis.

7.19 The thesis shall be adjudicated by an external examiner appointed by the Principal. For this, the COE shall submit a panel of **three** examiners from among the list of experts in the relevant specialization as submitted by the Head of the Department..

7.20 If the report of the external examiner is unsatisfactory, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unsatisfactory again, the thesis shall be summarily rejected. Subsequent actions for such dissertations may be considered, only on the specific recommendations of the external examiner and /or DRC. No further correspondence in this matter will be entertained, if there is no specific recommendation for resubmission.

7.21 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Dissertation Viva-Voce examination. The Dissertation Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis. The candidate has to secure a minimum of 50% of marks in Dissertation Evaluation (Viva-Voce) examination.

7.22 If he fails to fulfill the requirements as specified in 7.21, he will reappear for the Dissertation Viva-Voce examination **only after three months**. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree, unless he is asked to revise and resubmit his Dissertation Work by the board within a specified time period (within **four** years from the date of commencement of his first year first semester).

7.23 The Dissertation Viva-Voce External examination marks must be submitted to the COE on the day of the examination.

7.24 **For mandatory non-credit Audit courses, a student has to secure 40 marks out of 100 marks (i.e.40% of the marks allotted) in the CIE for passing the subject/course. These marks should also be uploaded along with the CIE marks of other subjects.**

7.25 **No marks or letter grades shall be allotted for mandatory non-credit Audit Courses. Only Pass/Fail shall be indicated in Grade Card.**

8. RE-ADMISSION / RE-REGISTRATION:

8.1 Re-Admission for Discontinued Student

A student, who has discontinued the M.Tech. degree programme due to any reason whatsoever, may be considered for '**readmission**' into the same degree programme (with the same specialization) with the academic regulations of the batch into which he gets readmitted, with prior permission from the authorities concerned, subject to item 6.6.

8.2 If a student is detained in a subject (s) due to shortage of attendance in any semester, he may be permitted to **re-register** for the same subject(s) in the same category (core or elective group) or equivalent subject, if the same subject is not available, as suggested by the Board of Studies of that department, as and when offered in the subsequent semester(s), with the academic regulations of the batch into which he seeks re-registration, with prior permission from the authorities concerned, subject to item 3.2

8.3 **A candidate shall be given one chance to re-register and attend the classes for a maximum of two subjects in a semester**, if the internal marks secured by a candidate are less than 40% and failed in those subjects but fulfilled the attendance requirement. A candidate must re-register for failed subjects within four weeks of commencement of the class work and secure the required minimum attendance. In the event of the student taking this chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stand cancelled.

9. EXAMINATIONS AND ASSESSMENT GRADING SYSTEM

9.1 Grades will be awarded to indicate the performance of the student in each Theory Subject/Lab/ Mini Project with Seminar/Dissertation, based on the percentage of marks obtained (CIE + SEE) as specified in Item 7 above, and a corresponding Letter Grade shall be given.

9.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	Letter Grade (UGC Guidelines)	Grade Points
90% and above (≥ 90% , ≤ 100%)	O (Outstanding)	10
Below 90% but not less than 80% (≥ 80% , < 90%)	A^+ (Excellent)	9
Below 80% but not less than 70% (≥ 70% , < 80%)	A (Very Good)	8
Below 70% but not less than 60% (≥ 60% , < 70%)	B^+ (Good)	7
Below 60% but not less than 50% (≥ 50% , < 60%)	B (Average)	6
Below 50% (< 50%)	F (Fail)	0
Absent	Ab	0

9.3 A student obtaining **'F'** Grade in any Subject is deemed to have 'failed' and is required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted. In such cases, his Internal Marks (CIE Marks) in those subjects will remain as obtained earlier.

9.4 If a student has not appeared for the examinations, '**Ab**' Grade will be allocated to him for any subject and shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted.

9.5 A Letter Grade does not imply any specific marks percentage; it is only the range of percentage of marks.

9.6 In general, a student shall not be permitted to repeat any Subject/Course(s) only for the sake of 'Grade Improvement' or 'SGPA/CGPA Improvement'.

9.7 A student earns Grade Point (GP) in each Subject/Course, on the basis of the Letter Grade obtained by him in that Subject/Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/Course.

Credit Points (CP) = Grade Point (GP) x Credits

9.8 The student passes the Subject/Course only when he **gets GP≥6 (B Grade or above).**

9.9 The SGPA is calculated by dividing the Sum of Credit Points secured from ALL Subjects/ Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

$$\mathbf{SGPA\ (S_i) = \sum (C_i \times G_i) / \sum C_i}$$

Where C_i is the no. of credits of the i^{th} course and G_i is the GP scored in the i^{th} course.

9.10 The CGPA is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the II Semester onwards, at the end of each Semester, as per the formula

$$\mathbf{CGPA = \sum (C_i \times S_i) / \sum C_i}$$

where S_i is the SGPA of the i^{th} semester and C_i is the total no. of credits in that semester.

Illustration of calculation of SGPA					Illustration of calculation of CGPA			
Course /Subject	**Credits**	**Letter Grade**	**Grade Points**	**Credit Points**	**Sem.**	**Credits**	**SGPA**	**Credits x SGPA**
Course 1	3	A	8	3 x 8 = 24	Sem I	18	7	18 x 7= 126
Course 2	3	O	10	3 x 10 = 30	Sem II	18	6	18 x 6= 108
Course 3	3	B	6	3 x 6 = 18	Sem III	12	8	12 x 8 = 96
Course 4	3	B	6	3 x 6 = 18	Sem IV	20	8	20 x 8 = 160
Course 5	2	A^+	9	2 x 9 = 18				
Course 6	2	B	6	2 x 6 = 12				
Course 7	2	B	6	2 x 6 = 12				
Total	**18**			**132**	**Total**	**68**		**490**
SGPA = 132/18 = 7.33					**CGPA = 490/68 = 7.20**			

10 AWARD OF DEGREE AND CLASS

10.1 If a student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of **68** Credits (with CGPA>6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. degree in the chosen Branch of Engineering and Technology with the specialization that he was admitted into.

10.2 After a student has earned the requirements prescribed for the completion of the programme and is eligible for the award of M.Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.75
First Class	6.75≤CGPA<7.75
Second Class	6.00≤CGPA<6.75

A student with final CGPA (at the end of the **PGP) < 6.00** shall not be eligible for the Award of Degree.

11 WITH HOLDING OF RESULTS

If the student has not paid the dues, if any, to the Institute or if any case of indiscipline is pending against him, the results and degree of the student will be with held and he will not be allowed into the next semester.

12 GENERAL

12.1 **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

12.2 **Credit Point:** It is the product of grade point and number of credits for a course.

12.3 Wherever the words "he", "him", "his", occur in the regulations, they shall include "she", "her".

12.4 The academic regulation should be read as a whole for the purpose of any interpretation.

12.5 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Institution is final.

12.6 The Institution may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Institute.

13 MALPRACTICE

13.1 **Malpractice Prevention Committee:** The committee shall examine the student's malpractice and indiscipline cases occurred, while conducting the examinations and recommend appropriate punishment to the Academic Council after taking explanation from the student and concerned invigilator as per the malpractice rules mentioned below. The committee consists of

a) Controller of Examinations - Chairman

b) Addl. Controller of Examinations.- Convener

c) Subject Expert - Member

d) Head of the Department of which the student belongs to - Member

e) The Invigilator concerned - Member

13.2 **Malpractice Rules:** Disciplinary Action for Improper Conduct in Examinations

S. No.	Nature of Malpractices / Improper Conduct	Punishment
1(a)	Possesses or keeps accessible in examination hall, any paper, notebook, programmable calculators, cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which the student is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
1(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, the student will be handed over to the police and a case is registered against them.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the Principal.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from the examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from classwork and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations

		of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6	Refuses to obey the orders of the Addl. Controller of examinations / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the addl. Controller of examinations or any person on duty in or outside the examination hall of any injury to his person or to any of their relations whether by words, either spoken or written or by signs or by visible representation, assaults the addl. Controller of examinations, or any person on duty in or outside the examination hall or any of their relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical

		examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9	If a student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the principal for further action to award suitable punishment.	

COURSE STRUCTURE

M.Tech. (VLSI) – R22 Course Structure

(Applicable from the batch admitted during 2022-23 and onwards)

I – Semester								
S. No.	Course Code	Subject	POs	PSOs	Hours Per Week			Credits
					L	T	P	
1	22VLPC11	Digital System Design with FPGAs	1,2,3	1,2	3	-	-	3
2	22VLPC12	CMOS Analog IC Design	1,2,3	1,2	3	-	-	3
3	**Professional Elective – I**				3	-	-	3
	22VLPE11	Pattern Recognition and Machine Learning	1,2,3	1,2				
	22VLPE12	CMOS Mixed Signal Design	1,2,3	1,2				
	22VLPE13	Memory Technologies	1,2,3	1,2				
4	**Professional Elective – II**				3	-	-	3
	22VLPE14	Communication Buses & Interfaces	1,2,3	1,2				
	22VLPE15	ARM Microcontrollers	1,2,3	1,2				
	22VLPE16	Embedded Real Time Operating System	1,2,3	1,2				
5	22VLPC13	Digital System Design with FPGAs Lab	1,2,3	1,2	-	-	4	2
6	22VLPC14	CMOS Analog IC Design Lab	1,2,3	1,2	-	-	4	2
7	22MC11	Research Methodology & IPR	1,2,3	1,2	2	-	-	2
8	**Audit Course -I**				2	-	-	0
	22AC11	English for Research Paper Writing	1,2,3					
	22AC12	Disaster Management	1,2,3					
	22AC13	Sanskrit for Technical Knowledge	1,2,3					
	22AC14	Value Education	1,2,3					
TOTAL					**16**	**00**	**08**	**18**

II – Semester								
S. No.	Course Code	Subject	POs	PSOs	Hours Per Week			Credits
					L	T	P	
1	22VLPC21	Internet of Things	1,2,3	1,2	3	-	-	3
2	22VLPC22	System Verilog Test Benches using UVM	1,2,3	1,2	3	-	-	3
3	**Professional Elective – III**				3	-	-	3
	22VLPE21	VLSI Advanced Physical Design	1,2,3	1,2				
	22VLPE22	SoC Design	1,2,3	1,2				
	22VLPE23	Design for Testability	1,2,3	1,2				
4	**Professional Elective – IV**				3	-	-	3
	22VLPE24	Device Modeling	1,2,3	1,2				
	22VLPE25	RFIC Design	1,2,3	1,2				
	22VLPE26	Hardware and Software Co-Design	1,2,3	1,2				
5	22VLPC23	Internet of Things Lab	1,2,3	1,2	-	-	4	2
6	22VLPC24	VLSI Design Verification and Testing Lab	1,2,3	1,2	-	-	4	2
7	22VLPR21	Mini Project with Seminar	1,2,3	1,2	-	-	4	2
8	**Audit Course -II**				2	-	-	0
	22AC21	Constitution of India	1,2,3					
	22AC22	Pedagogy Studies	1,2,3					
	22AC23	Stress Management by Yoga	1,2,3					
	22AC24	Personality Development Through Life Enlightenment Skills	1,2,3					
TOTAL					**14**	**00**	**12**	**20**

III – Semester								
S. No.	Course Code	Subject	POs	PSOs	Hours Per Week			Credits
					L	T	P	
1	**Professional Elective – V**				3	-	-	3
	22VLPE31	Advanced Computer Architecture	1,2,3	1,2				
	22VLPC32	Nanomaterials & Nanotechnology	1,2,3	1,2				
	22VLPC33	Hardware Security	1,2,3	1,2				
2	**Open Elective**				3	-	-	3
	22OE31	Business Analytics	1,2,3					
	22OE32	Industrial Safety	1,2,3					
	22OE33	Operations Research	1,2,3					
	22OE34	Cost Management of Engineering projects	1,2,3					
	22OE35	Composite Materials	1,2,3					
3	22VLPR31	Dissertation Work Review-II	1,2,3		-	-	12	6
TOTAL					**06**	**00**	**12**	**12**

IV – Semester								
S. No.	Course Code	Subject	POs	PSOs	Hours Per Week			Credits
					L	T	P	
1	22VLPR41	Dissertation Work Review-III	1,2,3	1,2	-	-	12	6
2	22VLPR42	Dissertation Viva-Voce	1,2,3	1,2	-	-	28	14
TOTAL					**00**	**00**	**40**	**20**

I-SEMESTER SYLLABUS

DIGITAL SYSTEM DESIGN WITH FPGAS

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22VLPC11	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	exposes the design approaches using FPGAs	3	3	3	3	3
CO2	provide in depth understanding of clocked sequential circuits	3	3	3	3	3
CO3	exposes the design approaches of Sequential circuit	3	3	3	3	3
CO4	analyze test pattern generation techniques for fault detection	3	3	3	3	3
CO5	design fault diagnosis in sequential circuits	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, FPGAs-FPGA technology, architecture, virtex CLB and slice, FPGA Programming Technologies, Xilinx XC2000, XC3000, XC4000 Architectures, Actel ACT1, ACT2 and ACT3 Architectures. [TEXTBOOK-1]		
II		11
A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. [TEXTBOOK-2]		
III		4+6=10
Part A: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Controller (FSM) – Metastability, Synchronization, FSM Issues.		
Part B: Pipelining resources sharing, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]		
IV		9
Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model. Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm.		
V		9
Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.3]		
Textbooks		
1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications. 2. Fundamentals of Logic Design-Charles H.Roth,Jr. -5thEd.,Cengage Learning.		
References		
1. Logic Design Theory- N.N.Biswas, PHI. 2. Digital System Design using programmable logic devices- ParagK.Lala, BS publications		

CMOS ANALOG IC DESIGN

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22VLPC12	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	describe basic building blocks of CMOS analog ICs	3	3	3	3	3
CO2	construct approaches of current mirror circuits	3	3	3	3	3
CO3	carry out the design of operational amplifiers	3	3	3	3	3
CO4	determine the device dimensions of each MOSFETs involved	3	3	3	3	3
CO5	compare various comparators	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I	**MOS Devices and Modeling**	9
The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout,CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small- Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.		
II	**Analog CMOS Sub-Circuits**	11
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors- Current mirror with Beta Helper, Degeneration, Cascade current Mirror and Wilson Current Mirror,Currentand VoltageReferences,BandgapReference.		
III	**CMOS Amplifiers**	4+6=10
Part A: Inverters, Differential Amplifiers, Cascode Amplifiers		
Part B: Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures		
IV	**CMOS Operational Amplifiers**	9
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures		
V	**Comparators**	9
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.		

Textbooks

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

References

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

PATTERN RECOGNITION AND MACHINE LEARNING
(Professional Elective-I)

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22VLPE11	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	familiar the basics of pattern classes and functionality	3	3	3	3	3
CO2	construct the various linear models	3	3	3	3	3
CO3	use the different kernel methods	3	3	3	3	3
CO4	design the inference in graphical models	3	3	3	3	3
CO5	carry out design of mixture models	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I	**Introduction to Pattern recognition**	9
Mathematical Formulation and Basic Functional Equation, Reduction of Dimensionality, Experiments in Pattern Classification, Backward Procedure for Both Feature Ordering- and Pattern Classification, Suboptimal Sequential Pattern Recognition, Nonparametric Design of Sequential Pattern Classifiers, Analysis of Optimal Performance and a Multiclass Generalization		
II	**Linear Models**	9
Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares , Sequential learning, Regularized least squares, Multiple outputs , The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs.		
III	**Kernel Methods**	6+4=10
Part A: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression.		
Part B: Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplace approximation, Connection to neural networks.		
IV	**Graphical Models**	9
Bayesian Networks, Example: Polynomial regression, Generative models, Discrete variables, Linear-Gaussian models, Conditional Independence- Three example graphs, D-separation, Markov Random Fields -Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models.		
V	**Mixture Models and EM algorithm**	9
K-means Clustering-Image segmentation and compression, Mixtures of Gaussians-Maximum likelihood, EM for Gaussian mixtures, An Alternative View of EM- Gaussian mixtures revisited, Relation to K-means, Mixtures of Bernoulli distributions, EM for Bayesian linear regression, The EM Algorithm in General, Combining Models- Tree-based Models,		
Textbooks		
1. Sequential methods in Pattern Recognition and Machine Learning-K.S.Fu, Academic Press, volume no.52.		
References		
1. Pattern Classification- Richard o. Duda, Peter E. hart, David G. Stork, John Wiley& Sons, 2nd Ed., 2001.		

CMOS MIXED SIGNAL DESIGN
(Professional Elective-I)

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22VLPE12	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	analyze the switched capacitor circuits	3	3	3	3	3
CO2	illustrate the working and applications of phased lock loop	3	3	3	3	3
CO3	analyze the fundamentals of data converter	3	3	3	3	3
CO4	apply the concepts of Nyquist rate A/D converters	3	3	3	3	3
CO5	explain the oversampling converters	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I	**Switched Capacitor Circuits**	9
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.		
II	**Phased Lock Loop (PLL)**	9
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/ Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications		
III	**Data Converter Fundamentals**	6+4=10
Part A: DC and dynamic specifications, Quantization noise, Nyquist rate		
Part B: D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.		
IV	**Nyquist Rate A/D Converters**	9
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.		
V	**Oversampling Converters**	9
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.		
Textbooks		
1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002. 2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010. 3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013.		
References		
1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003 2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.		

MEMORY TECHNOLOGIES
(Professional Elective-I)

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22VLPE13	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	explain the concepts of random access memory technologies	3	3	3	3	3
CO2	discuss about volatile memories	3	3	3	3	3
CO3	distinguish the concepts of non-volatile memories	3	3	3	3	3
CO4	describe semiconductor memory reliability and radiation effects	3	3	3	3	3
CO5	illustrate various memory technologies	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I	**Random Access Memory Technologies**	9
Static Random-Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.		
II	**RAM Memory controllers**	10
DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs, SRAM and DRAM Memory controllers		
III	**Non-Volatile Memories**	5+4=9
PART-A: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs		
PART-B: Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.		
IV	**Advanced Memory Technologies and High-density Memory Packing Technologies:**	10
Ferroelectric Random-Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random-Access Memories (MRAMs), Experimental Memory Devices.		
V	**Testing and Reliability**	10
Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.		
Textbooks		
1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience 2. KiyooItoh, "VLSI memory chip design", Springer International Ed.		
References		
1. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability, PHI		

COMMUNICATION BUSES AND INTERFACES
(Professional Elective-II)

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22VLPE14	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	select a particular serial bus suitable for a particular application	3	3	3	3	3
CO2	employ the architecture of CAN and applications	3	3	3	3	3
CO3	illustrate PCIe revisions, space configuration and protocols	3	3	3	3	3
CO4	design peripherals that establish interface to serial bus	3	3	3	3	3
CO5	discuss the serial communication protocol	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Serial Busses - Physical interface, Data and Control signals, features, limitations and applications of RS232, RS485, I2C, SPI		
II		9
CAN - Architecture, Data transmission, Layers, Frame formats, applications		
III		6+4=10
Part A:PCIe - Revisions, Configuration space.		
Part B: Hardware protocols, applications		
IV		9
USB - Transfer types, enumeration, Descriptor types and contents, Device driver		
V		9
Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable		

Textbooks

1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2nd Edition Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable
2. Jan Axelson, "USB Complete", Penram Publications
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press

References

1. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.

ARM MICROCONTROLLERS
(Professional Elective-II)

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22VLPE15	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	construct the selection criteria of ARM processors	3	3	3	3	3
CO2	illustrate Arm Instruction Set	3	3	3	3	3
CO3	explore the ARM development towards functional capabilities	3	3	3	3	3
CO4	create ASM level program using the instruction set	3	3	3	3	3
CO5	prepare the Programming ARM Cortex M	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I	**ARM Embedded Systems**	9
RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.Registers, Current Program Status Register, Pipeline, Exceptions Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.		
II	**Introduction to the Arm Instruction Set**	9
Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.		
III	**Technical Details of ARM Cortex M Processors**	6+4=10
Part A: General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set.		
Part B: Block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance.		
IV	**Instruction SET of ARM Cortex M**	9
Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4- specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.		
V	**Floating Point Operations**	9
Operations About Floating Point Data, Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP. **Case Study:**		
Textbooks		
1.ARM System Developer's Guide Designing and Optimizing System Software by Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier Publications, 2004.		
References		
1. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu,		

EMBEDDED REAL TIME OPERATING SYSTEM
(Professional Elective-II)

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22VLPE106	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	explain the concepts of RTOS	3	3	3	3	3
CO2	formulate RTOS kernel is implemented	3	3	3	3	3
CO3	describe how the RTOS implements time management	3	3	3	3	3
CO4	discuss interrupts as well timers	3	3	3	3	3
CO5	evaluate real time operating systems like RT Linux	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I	**Introduction**	9
Introduction to UNIX/LINUX, Overview of Commands, File I/O, (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).		
II	**Real Time Operating Systems**	9
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.		
III		6+4=10
Part A: Pipes, Event Registers, Signals, Other Building Blocks		
Part B: Component Configuration, Basic I/O Concepts, I/O Sub System.		
IV	**Exceptions, Interrupts and Timers**	9
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.		
V	**Case Studies of RTOS**	9
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.		
Textbooks		
1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011.		
References		
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, TMH, 2007. 2. Advanced UNIX Programming, Richard Stevens. 3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh.		

DIGITAL SYSTEM DESIGN WITH FPGAs LAB

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22VLPC13	0	0	4	2

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	test logic gates	3	3	3	3	3
CO2	design combinational circuits	3	3	3	3	3
CO3	develop sequential circuits	3	3	3	3	3
CO4	analyze finite state machines	3	3	3	3	3
CO5	construct CMOS circuit schematics and their layouts	3	3	3	3	3

List of Experiments

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

Week	Title/Experiment
1	HDL code to realize all the logic gates
2	Design and Simulation of Full Adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3	Design of Combinational circuit using Decoders.
4	Design of Combinational circuit using encoder (without and with parity).
5	Design of Combinational circuit using multiplexer.
6	Design of 4 bit binary to gray converter using MUX or Decoders.
7	Design of Multiplexer/ De Multiplexer, comparator in all 3 styles.
8	Modelling of an Edge triggered and Level triggered FFs : D, SR, JK
9	Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
10	Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out using different FFs.
11	Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12	Design of 4- Bit Multiplier, Divider.
13	Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment
14	Implementing the above designs on FPGA kits.

Reference

1. Digital System Design with FPGAs Lab Manual, Department of ECE, CMRIT, Hyd.

CMOS ANALOG IC DESIGN LAB

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22VLPC14	0	0	4	2

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	design CMOS logic gates	3	3	3	3	3
CO2	explain CMOS combinational circuits	3	3	3	3	3
CO3	develop CMOS sequential circuits	3	3	3	3	3
CO4	construct CMOS amplifiers	3	3	3	3	3
CO5	implement the CMOS SRAM cell	3	3	3	3	3

List of Experiments

List of Experiments List of Experiments *(*Any six experiments from each part are to be conducted): Transistor Level implementation of CMOS circuits using (180nm/90nm/45nm/Fin FET 18nm Technology)

Week	Title/Experiment
PART – A : Digital CMOS VLSI Design	
1	CMOS Buffer
2	CMOS NAND / NOR gates.
3	CMOS XOR
4	CMOS AND/OR gates
5	CMOS 28T Full Adder
6	CMOS 4:1 Multiplexer
7	CMOS Latch
8	CMOS Combinational circuits
9	CMOS Pass transistor
10	CMOS Complex circuits
11	CMOS 2:4 Decoder
PART – B: Analog CMOS VLSI Design	
1	CMOS Inverter
2	CMOS Common Source amplifier
3	CMOS Common Drain amplifier
4	CMOS Single stage Differential amplifier
5	CMOS Operational amplifier
6	CMOS SRAM CELL
7	CMOS D Flip-flop
8	CMOS SR Flip-flop
9	CMOS JK Flip-flop
10	CMOS T Flip-flop
Reference	
1. CMOS ANALOG IC DESIGN Lab Manual, Department of ECE, CMRIT, Hyd.	

RESEARCH METHODOLOGY AND IPR
(Mandatory Course)

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22MC11	2	0	0	2

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	formulate research problem	3	3	3	3	3
CO2	analyze research related information	3	3	3	3	3
CO3	follow research ethics	3	3	3	3	3
CO4	perceive nature of IPR and its development	3	3	3	3	3
CO5	outline the patent right	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations		
II		9
Effective literature studies approaches, analysis, Plagiarism, Research ethics		
III		6+4=10
Part A: Effective technical writing, how to write report, Paper Developing a Research Proposal		
Part B: Format of research proposal, a presentation and assessment by a review committe		
IV		9
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.		
V		9
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs		

Textbooks

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students"
2. C.R. Kothari, Research Methodology, methods & techniques, 2nd edition, New age International publishers

References

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2000

ENGLISH FOR RESEARCH PAPER WRITING
(Audit Course-I)

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22AC11	2	0	0	0

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	write a technical report without any ambiguity & redundancy	3	3	3
CO2	illustrate how to criticize/highlight-findings avoid plagiarism	3	3	3
CO3	apply various techniques of research to discuss results	3	3	3
CO4	exhibit technical communication skills in documentation	3	3	3
CO5	demonstrate research/technical paper publication skills	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness		
II		11
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction		
III		6+4=10
Part A: Review of the Literature, Methods, Results		
Part B: Discussion, Conclusions, The Final Check		
IV		9
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature		
V		9
skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions		

Textbooks

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)

References

1. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
2. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook.
3. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

DISASTER MANAGEMENT
(Audit Course-I)

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22AC12	2	0	0	0

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	analyze impact of disasters	3	3	3
CO2	choose suitable disaster management mechanism	3	3	3
CO3	make use of appropriate measures for capacity building to reduce risks	3	3	3
CO4	develop strategies to cope up with disasters	3	3	3
CO5	build disaster management plan	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Understanding Disaster: Concept of Disaster - Different approaches- Concept of Risk - Levels of Disasters - Disaster Phenomena and Events (Global, national and regional) **Hazards and Vulnerabilities:** Natural and man-made hazards; response time, frequency and forewarning levels of different hazards - Characteristics and damage potential or natural hazards; hazard assessment - Dimensions of vulnerability factors; vulnerability assessment - Vulnerability and disaster risk - Vulnerabilities to flood and earthquake hazards		
II		11
Disaster Management Mechanism: Concepts of risk management and crisis managements - Disaster Management Cycle - Response and Recovery - Development, Prevention, Mitigation and Preparedness - Planning for Relief		
III		6+4=10
Part A: Capacity Building: Capacity Building: Concept - Structural and Nonstructural Measures Capacity Assessment		
Part B: Strengthening Capacity for Reducing Risk - Counter-Disaster Resources and their utility in Disaster Management - Legislative Support at the state and national levels		
IV		9
Coping with Disaster: Coping Strategies; alternative adjustment processes – Changing Concepts of disaster management - Industrial Safety Plan; Safety norms and survival kits - Mass media and disaster management.		
V		9
Planning for disaster management: Strategies for disaster management planning - Steps for formulating a disaster risk reduction plan - Disaster management Act and Policy in India Organizational structure for disaster management in India - Preparation of state and district, Disaster management plans.		
Textbooks		
1. Manual on Disaster Management, National Disaster Management, Agency Govt of India. 2. Disaster Management by Mrinalini Pandey Wiley 2014. 3. Disaster Science and Management by T. Bhattacharya, TMH, 2015		
References		
1. 1. Earth and Atmospheric Disasters Management, N. Pandharinath, CK Rajan, BSP 2009. 2. National Disaster Management Plan, Ministry of Home affairs, Government of India (http://www.ndma.gov.in/images/policyplan/dmplan/draftndmp.pdf)		

SANSKRIT FOR TECHNICAL KNOWLEDGE
(Audit Course-I)

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22AC13	2	0	0	0

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	identify the alphabets	3	3	3
CO2	categorize past/present/future tenses	3	3	3
CO3	determine the roots of the language	3	3	3
CO4	relate the technical information about sanskrit language	3	3	3
CO5	articulate technical concepts of engineering	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Alphabets in Sanskrit		
II		11
Past/Present/Future Tense, Simple Sentences		
III		6+4=10
Part A: Order		
Part B: Introduction of roots		
IV		9
Technical information about Sanskrit Literature		
V		9
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics		

Textbooks

1. "Abhyaspustakam" – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit sansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

VALUE EDUCATION
(Audit Course-I)

Course	M.Tech.-I-Sem.	L	T	P	C
Subject Code	22AC14	2	0	0	0

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	interpret moral values, ethics, code of conduct and culture	3	3	3
CO2	illustrate humanity, honesty, devotion, confidence and patriotism	3	3	3
CO3	develop positive thinking, integrity and group cohesiveness	3	3	3
CO4	exhibit friendship, love for truth, and eco-friendly to environment	3	3	3
CO5	identify need for reincarnation, self-control and gender Equity	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements		
II		11
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline		
III		6+4=10
Part A: Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness		
Part B: Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance		
IV		9
True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature		
V		9
Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively		
Textbooks		
1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi		

II-SEMESTER SYLLABUS

INTERNET OF THINGS

Course	M.Tech.-II-Sem.	L	T	P	C
Subject Code	22VLPC21	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	explain the concept of internet of things and characteristics	3	3	3	3	3
CO2	describe the M2M with necessary protocols	3	3	3	3	3
CO3	discuss about python scripting language	3	3	3	3	3
CO4	compare IoT architectures	3	3	3	3	3
CO5	examine various types of case studies and IOT applications	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Introduction and definition of IoT, Evolution of IoT, IoT growth, Application areas of IoT, Characteristics of IoT, IoT stack, Enabling technologies, IoT levels, IoT sensing and actuation, Sensing types, Actuator types		
II		9
M2M to IoT – A Basic Perspective– Introduction, Differences and similarities between M2M and IoT, SDN and NFV for IoT.M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies.		
III		6+4=10
Part A: Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino		
Part B: Introduction to Python programming, Introduction to Raspberry Pi, Interfacing Raspberry Pi with basic peripherals, Implementation of IoT with Raspberry Pi.		
IV		9
IoT Architecture components, Comparing IoT architectures, A simplified IoT architecture, The core IoT functional stack, IoT data management and compute stack		
V		9
Challenges associated with IoT, Emerging pillars of IoT, Agricultural IoT, Vehicular IoT, Healthcare IoT, Smart cities, Transportation and logistics.		
Textbooks		
1. SudipMisra, Anandarup Mukherjee, Arijit Roy "Introduction to IOT", Cambridge University Press. 2. David Hanes, Gonzalo salgueiro, Patrick Grossetete, Rob barton, Jerome henry "IoT Fundamentals Networking technologies, protocols, and use cases for IoT", Cisco Press		
References		
1. Cuno pfister, "Getting started with the internet of things", O Reilly Media, 2011 2. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything", 1st Edition, Apress Publications.		

SYSTEM VERILOG TEST BENCHES USING UVM

Course	M.Tech.-II-Sem.	L	T	P	C
Subject Code	22VLPC22	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	implement test bench programs using system Verilog	3	3	3	3	3
CO2	construct object-oriented programming concepts	3	3	3	3	3
CO3	develop random stimulus and SVAs using system Verilog	3	3	3	3	3
CO4	analyze UVM components and UVM phases	3	3	3	3	3
CO5	compose Modeling UVM transactions with all its features	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Introduction, Verification need, Test bench components, Directed versus random stimulus, Code coverage versus functional coverage, Types of code coverage, Verification plan and test plan.		
II		11
Introduction, Constructs, Interface and object-oriented programming concepts.		
III		4+6=10
Part A: Randomization, Functional coverage		
Part B: system Verilog assertions.		
IV		9
Introduction, UVM components and UVM Introduction, Constructs, Interface and object-oriented programming concepts.phases		
V		9
UVM component configuration and factory, Modelling UVM transactions, UVM sequence, Virtual sequencer, Component communication and UVM reporting.		
Textbooks		
1. Janic Bergeron, "Writing Testbenches: Functional Verification of HDL Models", 2nd Ed., Kluwer Academic Publishers, 2003. 2. Stuart Sutherland, Simon DavidMann and Peter Flake, "System Verilog for Design", 2nd Ed., Springer, 2006.		
References		
1. Reference Verification Methodology User Guide, Version 8.5.11 – Synopsis.		

VLSI ADVANCED PHYSICAL DESIGN
(Professional Elective – III)

Course	M.Tech.-II-Sem.	L	T	P	C
Subject Code	22VLPE21	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	conduct power and IR analysis and design power mesh	3	3	3	3	3
CO2	apply low power implementation techniques and UPF formats	3	3	3	3	3
CO3	verify whether the design meets the power intent in UPF	3	3	3	3	3
CO4	examine STA on chip variations	3	3	3	3	3
CO5	perform physical verification of LVS/DRC levels and fix issues	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Introduction to power analysis, Goals and objectives, Data preparation, Power mesh design, Static IR analysis, Dynamic IR analysis, Signal and power EM.		
II		11
Introduction, Low power optimization in the SOC flow, Special cells for power management, Architectural techniques for low power.		
III		4+6=10
Part A: Low power implementation techniques (multi voltage, power gating etc.)		
Part B:UPF formats, Low power checks.		
IV		9
Hierarchical STA (ILM, XILM, ETM), On-chip variations, Advanced on-chip variations, Parametric on chip variations, Introduction to LVF.		
V		9
Physical verification - Introduction, goals and objectives, design rule check, layout versus schematic check and electrical rule check, Design for manufacturability - Introduction, DFM aware routing, DFM checks and fixing (pattern matching, MAS).		
Textbooks		
1. Rakesh Chadha and J. Bhasker, "An ASIC Low Power Primer", Springer, 2013.		
References		
1. Voltus Reference Manuals, 17.12.000. 2. Tempus Reference Manual, 17.12.000. 3. Calibre Reference Manual, 2017.1_17.12		

SOC DESIGN
(Professional Elective – III)

Course	M.Tech.-II-Sem.	L	T	P	C
Subject Code	22VLPE22	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	explain basic concept of ASIC	3	3	3	3	3
CO2	discuss about NISC	3	3	3	3	3
CO3	illustrate the basic concepts Simulation	3	3	3	3	3
CO4	describe Low power SoC design	3	3	3	3	3
CO5	make use of Synthesis	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.		
II		11
NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.		
III		4+6=10
Part A: Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors		
Part B: Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.		
IV		9
Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.		
V		9
Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report, analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption.		
Textbooks		
1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008. 2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006		
References		
1. Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000 2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008		

DESIGN FOR TESTABILITY
(Professional Elective – III)

Course	M.Tech.-II-Sem.	L	T	P	C
Subject Code	22VLPE23	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	discuss the Scope of testing and verification in VLSI design process	3	3	3	3	3
CO2	explain Fundamentals of VLSI testing and scan based design	3	3	3	3	3
CO3	analyze BIST for testing of logic and memories	3	3	3	3	3
CO4	design test automation for functional verification	3	3	3	3	3
CO5	describe about Testing Models	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, and Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.		
II		11
Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.		
III		4+6=10
Part A: SCOAP Controllability and Observability, High Level Testability Measures		
Part B: Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan		
IV		9
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.		
V		9
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.		
Textbooks		
1. M.L. Bushnell, V. D. Agrawal, "Essential of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits", Kluwer Academic Publishers.		
References		
1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design", Jaico Publishing House. 2. P. K. Lala, "Digital Circuits Testing and Testability", Academic Press		

DEVICE MODELLING
(Professional Elective – IV)

Course	M.Tech.-II-Sem.	L	T	P	C
Subject Code	22VLPE24	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	explain MOS contacts and modes of operations	3	3	3	3	3
CO2	describe the behavior of capacitor characteristics.	3	3	3	3	3
CO3	analyze small signal modeling	3	3	3	3	3
CO4	perform the switching characteristics the VLSI circuits	3	3	3	3	3
CO5	use the FinFET for various applications	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Mid gap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation		
II		11
CV characteristics of MOS, LFCV and HFCV, Non- idealities in MOS, oxide fixed charges, interfacial charges.		
III		4+6=10
Part A:CV characteristics of MOS, LFCV and HFCV.		
Part B: Pao-Sah and Brews models; Short channel effects in MOS transistors.		
IV		9
Eber's-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics.		
V		9
I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices.		
Textbooks		
1. S. M. Sze, "Physics of Semiconductor Devices", 2nd Ed., Wiley Eastern, 1981. 2. Y. P. Tsividis, "Operation and Modelling of the MOS Transistor", McGraw-Hill, 1987.		
References		
1. E. Takeda, "Hot-carrier Effects in MOS Transistors", Academic Press, 1995. 2. P. Colinge, "FinFETs and Other Multi-Gate Transistors", Springer. 2009		

RF IC DESIGN
(Professional Elective – IV)

Course	M.Tech.-II-Sem.	L	T	P	C
Subject Code	22VLPE25	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	analyze the behavior of high frequency components	3	3	3	3	3
CO2	illustrate various forms of RF filter design	3	3	3	3	3
CO3	implement component modelling and biasing networks	3	3	3	3	3
CO4	examine of RF transistor amplifier design	3	3	3	3	3
CO5	design the various RF filters, oscillators and mixers	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I	**Introduction**	8
Importance of RF design dimensions and units frequency spectrum RF behavior of passive components, high frequency resistors, high frequency capacitors, high frequency inductor, chip components and circuit board Considerations chip resistors chip capacitors and surface mount inductors.		
II	**RF filter design**	7
Scattering parameters: definition, meaning chain, scattering matrix, conversion between S- and Z-parameters, signal flow chart modeling, generalization basic resonator and filter configurations: low pass, high pass, band pass and band stop type filters-filter implementation using unit element and kuroda's identities transformations-coupled filters		
III	**Active RF component modeling RF filter design**	9+9=18
Part-A: RF diode models: nonlinear and linear models transistor models: large signal and small signal BJT models.		
Part-B:large signal and small signal FET models-scattering parameters device characterization		
IV	**RF transistor amplifier design**	8
Characteristics of amplifier-amplifier power relations RF sources, transducers power gain, additional power relations-stability consideration: stability circles, unconditional stability and stabilization methods-unilateral and bilateral design for constant gain noise figure circles- constant VSWR circles.		
V	**RF oscillators and mixers**	7
Basic oscillator models: Negative resistance oscillator, feedback oscillator design, design steps, quads oscillators- fixed frequency, And high frequency oscillator- basic characteristics of mixers: concepts, frequency domain considerations, single ended mixer design, single and double balanced mixers.		
Textbooks		
1. RF circuit design- theory and applications - Reinhold Ludwig Pavel bsetchko- Pearson education India 2000 2. Radio frequency and microwave communication circuits- analysis and design- devendrak Mishra- wiley student edition- john wiley and sons inc		
References		
1. Radiofrequency and microwave electronics mathew m rarmaneah PEI 2. RF circuit design christoper BOWIK Cheryl aijuni and john butler Elsevier science 2008 3. Secrets of RF circuit design joseph jcarr TMH 2000		

HARDWARE AND SOFTWARE CO-DESIGN
(Professional Elective – IV)

Course	M.Tech.-II-Sem.	L	T	P	C
Subject Code	22VLPE26	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	acquire the knowledge on various models of co-design	3	3	3	3	3
CO2	analyze prototyping and target architectures	3	3	3	3	3
CO3	compile tools for embedded processor architectures	3	3	3	3	3
CO4	compare techniques of design specification and verification	3	3	3	3	3
CO5	implement validation methods and adaptability	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I	**Co-Design Issues**	9
Co- Design Models, Architectures, Languages, A Generic Co-Design Methodology **Co-Synthesis Algorithms:** Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.		
II	**Prototyping and Emulation**	10
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.		
III	**Compilation techniques and tools for embedded processor architectures**	5+5=10
Part-A: Modern embedded architectures, embedded software development needs		
Part-B: Compilation technologies, practical consideration in a compiler development environment.		
IV	**Design Specification and Verification**	9
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.		
V	**Languages for System – Level Specification and Design-I**	10
System – level specification, design representation for system level synthesis, system level specification languages. **Languages for System – Level Specification and Design-II:** Heterogeneous specifications and multi- language co-simulation, the cosyma system and lycos system.		
Textbooks		

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, Kluwer Academic Publishers, 2002.

INTERNET OF THINGS LAB

Course	M.Tech.-II-Sem.	L	T	P	C
Subject Code	22VLPC23	0	0	4	2

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	improve working on basic IoT devices	3	3	3	3	3
CO2	determine learning and utilization of IoT devices	3	3	3	3	3
CO3	develop automation work-flow in IoT enabled environment	3	3	3	3	3
CO4	recommend working on advance IoT Systems	3	3	3	3	3
CO5	test remote IoT systems in the interest of society	3	3	3	3	3

List of Experiments

Week	Title/Experiment
1	Start Raspberry Pi and various Linux commands in command terminal window: ls, cd, touch, mv, rm, man, mkdir, rmdir, tar, gzip, cat, more, less, ps, sudo, cron, chown, chgrp, ping etc.
2	Python programs on Pi like: Read your name and print Hello message with name Read two numbers and print their sum, difference, product and division. Word and character count of a given string Area of a given shape (rectangle, triangle and circle) reading shape and appropriate values from standard input Print a name ‘n’ times, where name and n are read from standard input, using for and while loops. Handle Divided by Zero Exception. Print current time for 10 times with an interval of 10 seconds .Read a file line by line and print the word count of each line.
3	Write a program on Light an LED.
4	Write a program on input from two switches and switch on corresponding LEDs
5	Write a program on Flash an LED at a given on time and off time cycle, where the two times are taken from a file.
6	Write a program on Flash an LED based on cron output (acts as an alarm)
7	Write a program on Switch on a relay at a given time using cron, where the relay’s contact terminals are connected to a load.
8	Write a program on Access an image through a Pi web cam.
9	Write a program on Control a light source using web page.
10	To interface Bluetooth with Raspberry Pi and write a program to send sensor data to smart phone using Bluetooth
11	Write a program on Raspberry Pi to publish temperature data to MQTT broker.
12	Write a program on Raspberry Pi to subscribe to MQTT broker for temperature data and print it.
Reference	
1. Internet of Things Lab Manual, Department of ECE, CMRIT, Hyd.	

VLSI DESIGN VERIFICATION AND TESTING LAB

Course	M.Tech.-II-Sem.	L	T	P	C
Subject Code	22VLPC24	0	0	4	2

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	simulate different classes and loops in System Verilog	3	3	3	3	3
CO2	test and verify Front-End-Design in different environments	3	3	3	3	3
CO3	verify efficiency and effectiveness of complex designs	3	3	3	3	3
CO4	analyze, design and simulate digital circuits	3	3	3	3	3
CO5	apply CAD tools for the design of digital circuits	3	3	3	3	3

List of Experiments

Week	Title/Experiment
1	Different classes in System Verilog
2	Different Loops in System Verilog
3	Random number functions
4	Pre-randomize and post -randomize functions
5	Single Port RAM Synchronous Read/Write
6	Synchronous/Asynchronous FIFO
7	Asynchronous/Synchronous reset D- FF
8	Semaphore
9	Mailbox
10	Parity
11	Device under Test
12	UART Scoreboard

Reference

1. VLSI Design Verification And Testing Lab Manual, Department of ECE, CMRIT, Hyd,

MINI PROJECT WITH SEMINAR

Course	M.Tech.-II-Sem.	L	T	P	C
Subject Code	22VLPR21	0	0	4	2

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	identify the problem, assess the scope and develop a prototype	3	3	3	3	3
CO2	execute the project using modern tools	3	3	3	3	3
CO3	develop project report along with its scalability	3	3	3	3	3
CO4	exhibit project management skills	3	3	3	3	3
CO5	make use of engineering knowledge for societal sustenance	3	3	3	3	3

Guidelines

S.No	Title
The objective of the Mini Project with Seminar is to imbibe students with technical, analytical and innovative ideas to facilitate with theoretical and practical learning pertaining to relevant domain of interest. An individual student work under the guidance / mentorship of a departmental faculty with the aim of addressing solution to real world / societal problems using various R & D techniques.	
1	Students should start the Mini project with seminar under approved internal guide immediately after M.Tech. I Semester SEE and complete before M.Tech. II Semester SEE in any reputed organization without effecting regular classwork.
2	The students have to obtain NOC from both HOD and submit the same to the guide for commencement of Mini project with seminar.
3	Survey and study of published literature on the approved / assigned topic.
4	Perform Analysis/Modeling/Simulation/Experiment/Design/Feasibility/study test-facility.
5	The guide periodically monitors the performance of the student.
6	A candidate is permitted to register for the Mini project with Seminar after satisfying the attendance requirement in all the subjects, both theory and laboratory in I semester.
7	There shall be Mini Project with Seminar during II semester for CIE of 100 marks.
8	Mini Project with Seminar Viva Voce will be evaluated by the supervisor for 50 marks and DRC for another 50 marks.
9	Student shall carryout the mini project in consultation with the mini project supervisor which may include critically reviewing the literature, project implementation and submit it to the department in the form of a report and shall make a presentation before the DRC.
10	The student has to secure a minimum of 50% of marks in i) seminar presentation and ii) mini project viva voce, to be declared successful. If he fails to obtain the minimum marks, he has to reappear for the same as and when scheduled.

Evaluation Procedure

CIE Supervisor: 50 Marks		CIE DRC: 50 Marks		Total CIE: 100 Marks	
Item	**Marks**	**Item**	**Marks**	**Item**	**Marks**
Abstract & Scope	05	Abstract & Scope	05	Abstract & Scope	10
Research Design	05	Research Design	05	Research Design	10
Tools Used	05	Tools Used	05	Tools Used	10
Algorithm/Code	10	Algorithm/Code	10	Algorithm/Code	20
Execution & Test Run	10	Execution &Test Run	10	Execution & Test Run	20
Report	10	Report	10	Report	20
Q & A	05	Q & A	05	Q & A	10
Total	**50**	**Total**	**50**	**Total**	**100**

CONSTITUTION OF INDIA
(Audit Course-II)

Course	M.Tech.- II-Sem.	L	T	P	C
Subject Code	22AC21	2	0	0	0

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	illustrate origin, history and philosophy behind Indian constitution	3	3	3
CO2	explain various constitutional rights and duties	3	3	3
CO3	summaries the governance and legal administrative procedures	3	3	3
CO4	recognize the need for local self government and administration	3	3	3
CO5	identify importance of ECI and election of public representatives	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working) Philosophy of the Indian Constitution: Preamble Salient Features		
II		11
Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality Right to Freedom Right against Exploitation Right to Freedom of Religion Cultural and Educational Rights Right to Constitutional Remedies Directive Principles of State Policy Fundamental Duties.		
III		6+4=10
Part A: Organs of Governance: Parliament Composition Qualifications and Disqualifications Powers and Functions Executive President Governor Council of Ministers Judiciary		
Part B: Appointment and Transfer of Judges, Qualifications Powers and Functions		
IV		9
Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: ZilaPachayat. Elected officials and their roles, CEO ZilaPachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy		
V		9
Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.		
Textbooks		
1. The Constitution of India, 1950 (Bare Act), Government Publication		
References		
1. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015. 2. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014. 3. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015		

PEDAGOGY STUDIES
(Audit Course-II)

Course	M.Tech.- II -Sem.	L	T	P	C
Subject Code	22AC22	2	0	0	0

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	identify need right pedagogy in light of OBE	3	3	3
CO2	illustrate various modern pedagogical techniques in practice	3	3	3
CO3	interpret various techniques for evaluation and assessment	3	3	3
CO4	analyze the process of learning among stakeholder ecosystems	3	3	3
CO5	implement R&D for use of modern pedagogy with use of ICT	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.		
II		11
Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.		
III		6+4=10
Part A: Evidence on the effectiveness of pedagogical practices, Methodology for the indepth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change.		
Part B: Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.		
IV		9
Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes		
V		9
Research gaps and future directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.		
Textbooks		

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

STRESS MANAGEMENT BY YOGA
(Audit Course-II)

Course	M.Tech.- II -Sem.	L	T	P	C
Subject Code	22AC23	2	0	0	0

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	explain need for yoga to control stress	3	3	3
CO2	distinguish yam and niyam applications in real life	3	3	3
CO3	demonstrate methods of lifestyle and work balance	3	3	3
CO4	identify need for physical and mental fitness through yoga	3	3	3
CO5	apply principles and methods of yoga for a complete professional	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Definitions of Eight parts of yoga. (Ashtanga)		
II		11
Yam and Niyam.		
III		6+4=10
Part A: Do`s and Don't's in life. i) Ahinsa, satya, astheya, bramhacharya and aparigraha		
Part B: ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan		
IV		9
Asan and Pranayam		
V		9
i) Various yoga poses and their benefits for mind & body ii) Regularization of breathing techniques and its effects-Types of pranayam		
Textbooks		
1. 'Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur 2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata		

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTMENT SKILLS
(Audit Course-II)

Course	M.Tech.-II -Sem.	L	T	P	C
Subject Code	22AC24	2	0	0	0

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	interpret holistic development by neethi satakam sukthis	3	3	3
CO2	explain holistic development and its impact on personality	3	3	3
CO3	illustrate the importance of duties and responsibilities	3	3	3
CO4	explain the term, knowledge, mastery and role model behavior	3	3	3
CO5	exhibit glimpses of bhagavadgita in real life	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Neetisatakam-Holistic development of personality • Verses- 19,20,21,22 (wisdom) • Verses- 29,31,32 (pride & heroism) • Verses- 26,28,63,65 (virtue)		
II		11
Neetisatakam-Holistic development of personality • Verses- 52,53,59 (dont's) • Verses- 71,73,75,78 (do's)		
III		6+4=10
Part A: Approach to day to day work and duties. • Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48,		
Part B: • Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35, • Chapter 18-Verses 45, 46, 48.		
IV		9
Statements of basic knowledge. • Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 • Chapter 12 -Verses 13, 14, 15, 16,17, 18 • Personality of Role model. Shrimad Bhagwad Geeta:		
V		9
• Chapter2-Verses 17, Chapter 3-Verses 36,37,42, • Chapter 4-Verses 18, 38,39 • Chapter18 – Verses 37,38,63		
Textbooks		
1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata. 2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.		

III-SEMESTER SYLLABUS

ADVANCED COMPUTER ARCHITECTURE
(Professional Elective – V)

Course	M.Tech.-III-Sem.	L	T	P	C
Subject Code	22VLPE31	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	illustrate the instruction set, memory addressing of computer	3	3	3	3	3
CO2	handle the issues in pipelining and parallelism	3	3	3	3	3
CO3	level parallelism the hardware and ILP software approach	3	3	3	3	3
CO4	compare multiprocessors and thread level parallelism	3	3	3	3	3
CO5	familiarize the practical issues in inter network	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I	**Fundamentals of Computer Design**	9
Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.		
II	**Pipelines &Memory Hierarchy Design**	11
Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory		
III	**Instruction Level Parallelism the Hardware Approach and Multi Processors and Thread Level Parallelism**	4+6=10
Part A: Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach		
Part B: Branch prediction, high performance instruction delivery- hardware based speculation.		
IV	**Multi Processors and Thread Level Parallelism:**	9
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.		
V	**Inter Connection and Networks and Intel Architecture**	9
Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. **Intel Architecture:** Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls		
Textbooks		
1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, Elsevier.		
References		
1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design: Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw-Hill 2. Kai Hwang, Faye A.Brigs., "Computer Architecture and Parallel Processing", Mc Graw Hill		

NANOMATERIALS AND NANOTECHNOLOGY
(Professional Elective – V)

Course	M.Tech.-III-Sem.	L	T	P	C
Subject Code	22VLPE32	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	discuss the types of nanomaterials.	3	3	3	3	3
CO2	relate nano-materials for different applications	3	3	3	3	3
CO3	examine MEMS and quantum dots	3	3	3	3	3
CO4	propose carbon nanotubes for memories.	3	3	3	3	3
CO5	organize nano electronics for quantum computers	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies, Nano dimensional Materials 0D, 1D, 2D structures , Size Effects, Fraction of Surface Atoms, Specific Surface Energy and Surface Stress, Effect on the Lattice Parameter, Phonon Density of States, the General Methods available for the Synthesis of Nanostructures.		
II		11
Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional, nanomaterials, Two-dimensional nanomaterials, Three dimensional nanomaterials, Low-Dimensional Nanomaterials and its Applications, Synthesis, Properties, and Applications of Low-Dimensional Carbon-Related Nanomaterials		
III		4+6=10
Part A: Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS).		
Part B: Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding.		
IV		9
CNTs: Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT's, Multi-walled nanotubes, Single-walled nanotubes, Optical properties of CNT's, Electrical transport in perfect nanotubes, Applications as case studies, Synthesis and Applications of CNT's.		
V		9
Ferroelectric materials, coating, molecular electronics and nanoelectronics, biological and environmental, membrane based application, polymer based application		
Textbooks		
1. I Gusev and A ARempel, "Nanocrystalline Materials", Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008. 2. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, "Nanoscience and Nanotechnology", Tata McGraw Hill Education 2012..		
References		
1. Kenneth J. Klabunde and Ryan M. Richards, "Nanoscale Materials in Chemistry", 2 edition, John Wiley and Sons, 2009. 2. BharatBhushan, "Springer Handbook of Nanotechnology", Springer, 3rd edition, 2010.		

HARDWARE SECURITY
(Professional Elective – V)

Course	M.Tech.-III-Sem.	L	T	P	C
Subject Code	22VLPE33	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	describe counter-measures of various hardware attacks	3	3	3	3	3
CO2	experiment the impressive efficiency of hardware attacks	3	3	3	3	3
CO3	illustrate side channel attacks and mitigate risk of attacks	3	3	3	3	3
CO4	analyze silicon security and trust assessment for SoCs	3	3	3	3	3
CO5	design secure systems to privilege escalation and compromise	3	3	3	3	3

Syllabus

Unit	Title/Topics	Hours
I	**Introduction to Hardware Security**	10
Overview of the computing system, Layers of computing system, Hardware security vs hardware trust, Attacks, Vulnerabilities and counter measures, Conflict between security and Test/Debug, Evolution of Hardware security, Birds eye view, Common hardware security primitives, Performance reliability vs security, Security architecture		
II	**Hardware Trojans**	10
Introduction, SoC design flow, Hardware Trojans, Hardware Trojans in FPGA designs, Hardware Trojans taxonomy, Trust benchmarks, Countermeasures against Hardware Trojans, Software induced hardware Trojan attacks.		
III	**Side-Channel Attacks**	4+5=9
Part-A: Introduction, Background on side-channel attacks, Power analysis attacks, Electromagnetic side-channel attacks.		
Part-B: Fault injection attacks, Timing attacks, Covert channels, Side channel resistant design, Software induced side channel attacks.		
IV	**Test Oriented Attacks**	10
Amplitude amplification, Quantum Fourier Transform, Phase Kick-back, Quantum Phase estimation, Quantum Walks.		
V	**Physical Attacks and Counter Measures**	9
Introduction, Reverse engineering, Probing attacks, Invasive fault injection attack, Security issues in IP based SoC design, Security issues in FPGA, PCB security challenges and attack modes.		
Textbooks		
1. SwarupBhunia, Mark Tehranipoor, "Hardware Security A hands on learning approach",, Morgan Kaufmann Publisher, An Imprint of Elsevier.. 2. Douglas R Stinson, "Cryptography: Theory and practice", CRC Press.		
References		
1. Alfread J Menezes, Paul C Van Oorschot, Vanstone, A. Scott "Handbook of applied Cryptography", CRCPress. 2. Stefan Mangard, Elisabeth Oswald, Thomas Popp, "Power analysis attacks: Revealing the secrets of smart cards", Springer-Verlag.		

BUSINESS ANALYTICS
(Open Elective)

Course	M.Tech.-III-Sem.	L	T	P	C
Subject Code	22OE31	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	identify and relate variables in business analytics	3	3	3
CO2	build a suitable statistical model through business analytics	3	3	3
CO3	apply predictive analytics and structure business analytics in organization	3	3	3
CO4	forecast variables/attributes and fit trend	3	3	3
CO5	analyze decisions in light of constraints	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.		
II		11
Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.		
III		4+6=10
Part A: Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, measuring contribution of Business analytics, Managing Changes. Descriptive Analytics		
Part B: Predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.		
IV		9
Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.		
V		9
Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making. Recent Trends in Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism		
Textbooks		
1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.		
References		
1. Business Analytics by James Evans, Pearsons Education.		

INDUSTRIAL SAFETY
(Open Elective)

Course	M.Tech.-III-Sem.	L	T	P	C
Subject Code	22OE32	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	summarize the industrial safety	3	3	3
CO2	explain the fundamentals of maintenance engineering	3	3	3
CO3	outline the prevention of wear and corrosion	3	3	3
CO4	determine the faults	3	3	3
CO5	illustrate periodic and preventive maintenance	3	3	3

Syllabus

Unit	Title/Topics	Hours
I	**Industrial safety**	9
Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.		
II	**Fundamentals of maintenance engineering**	11
Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.		
III	**Wear and Corrosion and their prevention**	4+6=10
Part A: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication		
Part B: Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.		
IV	**Fault tracing**	9
Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault-finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, i. Any one machine tool, ii. Pump iii. Air compressor iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.		
V	**Periodic and preventive maintenance**	9
Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: i. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, Advantages of preventive maintenance. Repair cycle concept and importance		
Textbooks		
1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services. 2. Maintenance Engineering, H. P. Garg, S. Chand and Company		
References		
1. Pump-hydraulic Compressors, Audels, McGraw Hill Publication. 2. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.		

OPERATIONS RESEARCH
(Open Elective)

Course	M.Tech.-III-Sem.	L	T	P	C
Subject Code	22OE33	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	illustrate various methods and techniques of or	3	3	3
CO2	formulate IBFS for any problem	3	3	3
CO3	apply methods of non-linear programming	3	3	3
CO4	solve problems of scheduling and sequencing	3	3	3
CO5	identify suitable decision and apply to real world problems	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models		
II		11
Formulation of a LPP - Graphical solution revised simplex method - duality theory – dual simplex method - sensitivity analysis - parametric programming		
III		4+6=10
Part A: Nonlinear programming problem - Kuhn-Tucker conditions		
Part B: Min cost flow problem – max flow problem - CPM/PERT		
IV		9
Scheduling and sequencing - single server and multiple server models – deterministic inventory models - Probabilistic inventory control models - Geometric Programming.		
V		9
Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation		
Textbooks		
3. H.A. Taha, Operations Research, An Introduction, PHI, 2008 4. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982. 5. J.C. Pant, Introduction to Optimization: Operations Research, Jain Brothers, Delhi, 2008		
References		
1. Hitler Libermann Operations Research: McGraw Hill Pub. 2009 2. Pannerselvam, Operations Research: Prentice Hall of India 2010 3. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010		

COST MANAGEMENT OF ENGINEERING PROJECTS
(Open Elective)

Course	M.Tech.-III-Sem.	L	T	P	C
Subject Code	22OE34	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	interpret different costing systems	3	3	3
CO2	summarize the elements of project	3	3	3
CO3	analyze cost behavior and profit planning	3	3	3
CO4	examine the budgets	3	3	3
CO5	illustrate quantitative techniques for cost management	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Introduction and Overview of the Strategic Cost Management Process Cost concepts in decision making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.		
II		11
Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre-project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process		
III		4+6=10
Part A: Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis.		
Part B: Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints.		
IV		9
Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.		
V		9
Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.		
Textbooks		
1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi 2. Charles T. Horngren and George Foster, Advanced Management Accounting		
References		
1. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting 2. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher 3. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.		

COMPOSITE MATERIALS
(Open Elective)

Course	M.Tech.-III-Sem.	L	T	P	C
Subject Code	22OE35	3	0	0	3

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3
CO1	classify composite materials	3	3	3
CO2	analyze reinforcements and mechanical behaviour of components	3	3	3
CO3	manufacture metal matrix composites and carbon composites	3	3	3
CO4	prepare polymer matrix composites	3	3	3
CO5	estimate the strength of composites	3	3	3

Syllabus

Unit	Title/Topics	Hours
I		9
Introduction: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.		
II		11
Reinforcements: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.		
III		4+6=10
Part A: Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites		
Part B: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications		
IV		9
Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.		
V		9
Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.		

Textbooks

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.
3. Hand Book of Composite Materials-ed-Lubin.

References

1. Composite Materials – K. K. Chawla.
2. Composite Materials Science and Applications - Deborah D. L. Chung.
3. Composite Materials Design and Applications - Danial Gay, Suong V. Hoa, and Stephen W. Tasi

DISSERTATION WORK REVIEW - II

Course	M.Tech.-III-Sem.	L	T	P	C
Subject Code	22VLPR301	0	0	12	6

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	identify the problem, assess the scope and develop a prototype	3	3	3	3	3
CO2	execute the project using modern tools	3	3	3	3	3
CO3	develop project report along with its scalability	3	3	3	3	3
CO4	exhibit project management skills	3	3	3	3	3
CO5	make use of engineering knowledge for societal sustenance	3	3	3	3	3

Guidelines

S.No	Title
1	Students should start the Dissertation Work Review (which would be monitored in two stages i.e., DWR-I and DWR-II) under approved internal guide immediately after M.Tech. II semester SEE and complete before M.Tech. III semester SEE.
2	Every candidate shall be required to submit a dissertation on a topic approved by the Dissertation Review Committee and present in DWR-I, in consultation with his Supervisor, the title, objective and plan of action of his Dissertation work to the DRC for approval within four weeks from the commencement of III Semester.
3	Only after obtaining the approval of DRC the student can initiate the Dissertation work.
4	If any candidate wishes to change their supervisor or topic of the dissertation, they can do so with the approval of the DRC. However, the date of registration for the project work starts from the date of change of supervisor or topic.
5	A candidate shall submit his Dissertation progress report in two stages at least with a gap of three Months between them.
6	The work on the dissertation shall be initiated at the beginning of the III semester and the duration of the Dissertation is two semesters. A candidate is permitted to submit Dissertation Thesis only after successful completion of all theory and practical courses with the approval of DRC. For the approval of DRC, the candidate shall submit the draft copy of thesis to the HOD and make a presentation before the DRC.
7	The Dissertation Work Review-II in III Semester carries 100 internal marks.
8	Evaluation should be done by the DRC for 50 marks and rest by the Supervisor.
9	The Supervisor and DRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Dissertation Work.
10	A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - II. If he fails to obtain the minimum required marks, he has to reappear for Dissertation Work Review-II as and when conducted next.

Evaluation Procedure					
CIE Supervisor: 50 Marks		CIE DRC: 50 Marks		Total CIE: 100 Marks	
Item	Marks	Item	Marks	Item	Marks
Abstract	05	Abstract	05	Abstract	10
Scope	05	Scope	05	Scope	10
Objectives	05	Objectives	05	Objectives	10
Literature Survey	10	Literature Survey	10	Literature Survey	20
Research Design	10	Research Design	10	Research Design	20
Report	10	Report	10	Report	20
Q & A	05	Q & A	05	Q & A	10
Total	**50**	**Total**	**50**	**Total**	**100**

IV-SEMESTER SYLLABUS

DISSERTATION WORK REVIEW - III

Course	M.Tech.-IV-Sem.	L	T	P	C
Subject Code	22VLPR41	0	0	12	6

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	identify the problem, assess the scope and develop a prototype	3	3	3	3	3
CO2	execute the project using modern tools	3	3	3	3	3
CO3	develop project report along with its scalability	3	3	3	3	3
CO4	exhibit project management skills	3	3	3	3	3
CO5	make use of engineering knowledge for societal sustenance	3	3	3	3	3

Guidelines

S.No	Title
1	Students should continue the Dissertation Work Review-III on approval of DWR-II and commence immediately after M.Tech. III semester SEE and submit after successful completion of all theory and lab courses.
2	The DWR-III in IV Sem. carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate it for the other 50 marks.
3	The DRC will examine the overall progress of the Dissertation Work and decide whether or not the Dissertation is eligible for final submission.
4	A candidate has to secure a minimum of 50% of marks to be declared successful in DWR - III. If he fails, he has to reappear for the same as and when offered.
5	Unless DWR - III successfully completed, no candidate allowed to appear for Dissertation Viva-Voce examination (SEE).
6	DWR-II and III shall be conducted in phase I (Regular) and Phase II (Supplementary).
7	These students shall reappear for DWR - III in the next academic year in the process above mentioned.
8	After approval from the DRC, a soft copy of the thesis should be submitted for ANTI-PLAGIARISM check and be included in the final thesis.
9	The Thesis will be accepted for submission, if the similarity index is less than **30%**. In case of any failure, the student should ascertain conformity and re-submit after a month. The candidate should attach the copy of plagiarism report in both soft and hard copies.
10	Three copies of the Dissertation Thesis certified by the supervisor shall be submitted to the department along with a copy of communication on research paper related to the Dissertation work in any UGC approved journal.

Evaluation Procedure

CIE Supervisor: 50 Marks		CIE DRC: 50 Marks		Total CIE: 100 Marks	
Item	**Marks**	**Item**	**Marks**	**Item**	**Marks**
Abstract & Scope	05	Abstract & Scope	05	Abstract & Scope	10
Research Design	05	Research Design	05	Research Design	10
Tools Used	05	Tools Used	05	Tools Used	10
Algorithm/Code	10	Algorithm/Code	10	Algorithm/Code	20
Execution & Test Run	10	Execution &Test Run	10	Execution & Test Run	20
Publication/ Report	10	Publication/ Report	10	Publication/ Report	20
Q & A	05	Q & A	05	Q & A	10
Total	**50**	**Total**	**50**	**Total**	**100**

DISSERTATION VIVA VOCE

Course	M.Tech.-IV-Sem.	L	T	P	C
Subject Code	22VLPR402	0	0	28	14

Course Outcomes (COs) & CO-PO Mapping (3-Strong; 2-Medium; 1-Weak Correlation)

COs	Upon completion of course the students will be able to	PO1	PO2	PO3	PSO1	PSO2
CO1	describe the problem, scope and research methodology	3	3	3	3	3
CO2	illustrate tools used	3	3	3	3	3
CO3	summarize the findings	3	3	3	3	3
CO4	outline inferences out of project	3	3	3	3	3
CO5	explain conclusions, recommendations and future scope	3	3	3	3	3

Guidelines

S. No.	Title
1	Dissertation Viva-Voce examination Evaluation in IV Semester is for 100 marks SEE.
2	The candidate has to secure a minimum of 50% marks in DVV SEE.
3	The DVV SEE shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner for adjudication.
4	If the report of the external examiner is unsatisfactory, the candidate shall revise and resubmit the Thesis as recommended by the committee and/or after three months.

Evaluation Procedure for SEE 100 Marks	
Description	**Marks**
Introduction	10
Literature Review	10
Tools Used	20
Algorithm and Execution	30
Report	10
Q & A	20
Total	**100**

CMR INSTITUTE OF TECHNOLOGY

UGC Autonomous

(Approved by AICTE, Affiliated to JNTUH, Accredited by NBA & NAAC with 'A' Grade)
Kandlakoya (V), Medchal District, Hyderabad-501 401
Phone: 08418 – 200720 / 9247605109 Fax: 08418 – 200240, www.cmritonline.ac.in

UNDERTAKING BY STUDENT/PARENT REGARDING R22 REGULATIONS

ACADEMIC YEAR: 20____ - 20____

College Code	**R0**										Affix recent Stamp Size Photograph
Course	I - M.Tech.										
Branch	VLSI										
Roll No.			R	0	1	D	5	7			
Student Name											
Fathers' Name											

Declaration

1. I am completely aware of academic regulations prescribed by CMR Institute of Technology from the Academic Year 2022-23 onwards under which I was admitted.
2. I am aware of course registration before commencement of each semester with help of faculty mentor/advisor/Head of the Department.
3. I am aware of attendance detention procedure/system and minimum attendance requirement, of 75% without condonation, to be promoted to the next academic semester/year.
4. I am aware of credit detention regulations and minimum credits to be earned by me to promote to next academic year.
5. Guidelines for Mini-Project with Seminar/Dissertation Work Review-II/ Dissertation Work Review-III/ Dissertation Viva Voce as per R22 Regulations.
6. I am aware that minimum marks required in Continuous Internal Evaluation (CIE) are 40% of 40 CIE i.e. 16 marks out of 40, minimum 40% of Semester End examination (SEE) for 60 marks i.e. 24 marks out of 60 and minimum 50% of total marks of 100 i.e. 50 marks out of 100 marks both CIE & SEE marks taken together.
7. Re-registration of course if marks in CIE are less than 40% of 40 marks to improve CIE marks. When this option is exercised, I will forego the marks of SEE if any.
8. Guidelines for re-admission from one regulation to readmitted year regulations.
9. Malpractice rules and punishment.
10. Punishment of ragging, if involved in ragging of any student(s).

Date		**Signature of the Student**		**Signature of the Parent**	

Endorsement by the Head of the concerned Department and Principal

Date		**Name of the Dept. Head**		**Signature**	
Date		**Name of the Principal**		**Signature**	
College Stamp					